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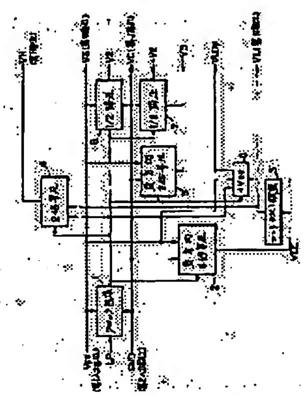
(54) POWER SOURCE CIRCUIT, LIQUID CRYSTAL DISPLAY DEVICE, AND ELECTRONIC EQUIPMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce power consumption of a liquid crystal display device relating to a power source circuit for supplying driving voltages of a liquid crystal VH, V3, V2, VC, −V2, −V3, VL, or the like.
SOLUTION: A charge-pump circuit performs charge-pump operation based on a clock generated by a latch pulse (a pulse-form clock including a periodically generated pulse), and supplies a driving potential of the liquid crystal. Charging of a pumping capacitor and a backup capacitor is halted for the LP pulse generation period. The charge-pump operation for alternately charging the backup capacitor by plural pumping capacitors is performed based on a given clock. Charging of the pumping capacitors and the backup capacitor are carried out in each horizontal scanning period in driving the liquid crystal.



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CLAIMS

[Claim(s)]

[Claim 1] It is the power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device – the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on the clock generated with the pulse-like clock including the pulse generated periodically, and supplies directly either [said] the 1st – the Nth potential through an adjustment means, The power circuit characterized by including a means to stop charge of the pumping capacitor which said charge pump circuit contains, and charge of the backup capacitor by the pumping capacitor during the nascent state of said pulse of said pulse-like clock.

[Claim 2] It is the power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device – the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly said 1st potential by the side of high potential, or said Nth potential by the side of low voltage through an adjustment means, Charge pump actuation which charges a backup capacitor by turns by two or more pumping capacitors is performed based on a given clock. The power circuit characterized by including the charge pump circuit which supplies directly the Ith potential in said 1st [the] – the Nth potential (1<I<N) through an adjustment means.

[Claim 3] It is the power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device – the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly either [said] the 1st – the Nth potential through an adjustment means, The power circuit characterized by including a means to make charge of the pumping capacitor which said charge pump circuit contains, and charge of the backup capacitor by the pumping capacitor perform for every 1 horizontal-scanning period in the drive of said display device.

[Claim 4] The power circuit where said charge pump circuit is characterized by performing charge pump actuation which charges a backup capacitor by turns for every 1 level period by two or more pumping capacitors in claim 3.

[Claim 5] The power circuit characterized by including a means to suspend the given clock of said charge pump circuit, in claim 1 thru/or either of 4.

[Claim 6] The liquid crystal display characterized by including the power circuit of claim 1 thru/or either of 5, the liquid crystal panel containing the liquid crystal layer driven with two or more data-line electrodes and two or more scanning-line electrodes, the data-line driver that drives said data-line electrode based on the potential supplied by said power circuit, and the scanning-line driver which drives said scanning-line electrode based on the potential supplied by said power circuit.

[Claim 7] The power circuit which an input power electrical potential difference is given and supplies the 1st – the Nth (N>=4) potential, The liquid crystal panel containing the liquid crystal layer driven with two or more data-line electrodes and two or more scanning-line electrodes, The data-line driver which drives said data-line electrode based on the potential supplied by said power circuit, It is a liquid crystal display containing the scanning-line driver which drives said scanning-line electrode based on the

potential supplied by said power circuit. A means by which said power circuit supplies the 1st input potential by the side of the high potential contained in said input power electrical potential difference, and the 2nd input potential by the side of low voltage as either [said] the 1st – the Nth potential, Based on a given clock, perform charge pump actuation, and the charge pump circuit which supplies directly either [said] the 1st – the Nth potential through an adjustment means is included. The liquid crystal display characterized by using said 1st and 2nd input potential as supply voltage of one [at least] logic section of said data-line driver and a scanning-line driver.
[Claim 8] The liquid crystal display characterized by including the charge pump circuit to which said power circuit generates the potential which differs from said 1st and 2nd input potential by charge pump actuation based on a given clock, and supplies this generating potential as either [said] the 1st – the Nth potential in claim 7.
[Claim 9] The power circuit which an input power electrical potential difference is given and supplies the 1st – the Nth (N>=4) potential, The liquid crystal panel containing the liquid crystal layer driven with two or more data-line electrodes and two or more scanning-line electrodes, The data-line driver which drives said data-line electrode based on the potential supplied by said power circuit, It is a liquid crystal display containing the scanning-line driver which drives said scanning-line electrode based on the electrical potential difference supplied by said power circuit. Said power circuit performs charge pump actuation based on the clock generated with the latch pulse for said data-line drivers, or the shift clock for said scanning-line drivers. The liquid crystal display characterized by including the charge pump circuit which supplies directly either [said] the 1st – the Nth potential through an adjustment means.
[Claim 10] Electronic equipment characterized by including the liquid crystal display of claim 6 thru/or either of 9.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the electronic equipment containing a liquid crystal display including a power circuit and this power circuit, and this liquid crystal display.
[0002]
Background Art and Problem(s) to be Solved by the Invention] As 1st background technique, the power circuit used for the liquid crystal display of an one-line line sequential drive is explained using drawing 48 . This drawing is fundamentally [as drawing 3 of JP,2-150819,A] the same. here — V0–V5 — VD=V0–V1=V1–V2=V3–V4=V4–V5 — having [for example,] relation, in the case of 1/240 duty, VD is about 1.6V.
[0003] The electrical potential difference inputted into a liquid crystal display from the outside is VEE

for making VCC and liquid crystal panel driver voltage for the logic section of a driver IC by making GND into a reference potential. VEE is quite high compared with VCC, for example, in the case of 1/240 duty, is about 20V-25V. VEE is used for V0 among V0-V5, and GND is used for V5 as it is. What carried out low impedance conversion of the electrical potential difference which divided between VEE-GND by resistance R1-R5 with operational amplifiers OP1-OP4 is used for V1 remaining-V4 remaining. OP1-OP4 operate on the electrical potential difference of a VEE system, and VCC is not participating in formation of the panel driver voltage itself directly.

[0004] Hereafter, a scanning-line side is expressed with Y, a data-line side is expressed with X, and power consumption is described. For example, the driver IC which drives [the driver IC which drives Y electrode and Y electrode for the scanning-line electrode of a panel] X electrode and X electrode for Y driver and the data-line electrode of a panel is expressed as X driver. The electrical potential difference applied to non-choosing Y electrode is V1 or V4. And when non-choosing Y electrode is V1, the electrical potential difference applied to X electrode is V0 or V2, and when non-choosing Y electrode is V4, the electrical potential difference applied to X electrode is V3 or V5.

[0005] In the case of 1/240 duty, all of the remaining 239 lines are in the condition of not choosing, to Y electrode of a selection condition being only one line. Therefore, the charge and discharge current which flows between X electrode and Y electrode of a selection condition is quite smaller than the charge and discharge current which flows between X electrode and Y electrode in the condition of not choosing. That is, the charge and discharge current to which the consumed electric current of the liquid crystal panel itself flows between X electrode and Y electrode in the condition of not choosing is most. Therefore, it observes only about the charge and discharge current which flows between X electrode and Y electrode in the condition of not choosing here.

[0006] For example, when the electrical potential difference of non-choosing Y electrode is V1, the case where the electrical potential difference of X electrode changes to V2 from V0 is considered. If capacity of a X-Y inter-electrode liquid crystal layer is set to Cpn at this time, in case the electrical potential difference of X electrode will be set to V1 from V0, the charge of Cpnx (V0-V1) flows out of V0, and flows into V1 (refer to D of drawing 48). Next, in case the electrical potential difference of X electrode is set to V2 from V1, the charge of Cpnx (V1-V2) flows out of V1, and flows into V2 (refer to E). Since it is V0-V1=V1-V2 here, the charge which flows into V1, and the charge which flows out of V1 become equal. Therefore, the outflow close of the charge of V1 serves as total zero, and as a result, the charge of Cpnx (V0-V2) will flow out of V0, and will flow into V2 (refer to F). Finally this charge flows into GND through an operational amplifier OP2 (refer to G). However, in the path in which the inside of OP2 is moved and it results to GND, this charge does not carry out effective work, but only generates heat loss, and becomes making OP2 generate heat. If the charge and discharge current of the panel in this case is set to Ipn and GND=0V, the power consumption by this Ipn will serve as IpnxVEE. And this rate of a deployment of Ipn is (V0-V2)/VEE so that clearly from G of drawing 48 . To V0-V2 being about 2x1.6V in the case of 1/240 duty, since VEE(s) are 20V-25V, it will be said that the rate of a deployment is 16% or less.

[0007] As 2nd background technique, the power circuit used for the liquid crystal display of a four-line coincidence selection drive is explained. The fundamental concept of the drive approach (MLS drive) which chooses two or more Y electrodes (line electrode) as coincidence is indicated by reference 1 (A GENERALIZED ADDRESSING TECHNIQUE FOR RMS RESPONDINGMATRIX LCDS the lecture collection of . 1988 INTERNATINAL DISPLAY RESEARCH CONF. 80-85 pages), and USP5,262,881. According to the MLS drive, this problem is solvable, although the fall of contrast becomes a problem when the response of liquid crystal is made quick by simple one-line line sequential drive.

[0008] When making coincidence selection of the L lines (L is two or more positive integers) by MLS drive, the potential of a total of three level of VH and VL which makes VM and this VM middle point potential is needed for Y electrode. VM is used for VH and non-choosing potential and VL are used for

selection potential here. Moreover, the potential of level (L+1) is needed for X electrode focusing on VM. Electrical-potential-difference width-of-face VH-HL which drives Y electrode becomes small, and big electrical-potential-difference width of face is needed for the drive of X electrode conversely as L becomes large.

[0009] An example of the power circuit considered when four-line coincidence sorting by selection is used for drawing 49 is shown. An electrical potential difference required for the drive of a panel is Vx0-Vx4 used as the driver voltage of VH and VL used as the selection electrical potential difference of Y electrode, VM used as the non-choosing electrical potential difference of Y electrode, and X electrode. VM serves as central potential of the electrical potential difference applied to a panel, and the relation of VH-VM=VM-VL and Vx0-Vx1=Vx1-Vx2=Vx2-Vx3=Vx3-Vx4 is realized. Moreover, the central potentials Vx2 by the side of X electrode are VM and this potential. For example, by the panel of 1/240 duty, VH-VL becomes about 25V and Vx0-Vx1 becomes about 1.6V.

[0010] The electrical potential difference inputted into a liquid crystal display from the outside makes GND a reference potential (0V), and it is VCC for the logic section of a driver IC, and VEE (= VH-VL) for making liquid crystal panel driver voltage, and as mentioned above, VEE is quite a high voltage compared with VCC. In addition, in drawing 4949 , VDDy and VSSy are the electrical potential differences of the logic section of Y driver, and connection of VCC and the GND is carried out as it is. Moreover, VDDx and VSSx are the electrical potential differences of the logic section of X driver, and are VDDx-VSSx=VCC as GND=0V. Pressure-proofing required for X driver is Vx0-Vx4, for example, can be managed with about 7V by the panel of 1/240 duty. VEE and GND are respectively used for VH and VL as it is. What carried out low impedance conversion of the electrical potential difference which divided between VEE-GND by resistance R1-R6 with operational amplifiers OP1-OP6 is used for Vx0-Vx4, and VSSX. Moreover, in order to materialize the relation of VDDx-VSSx=VCC, the resistance of R7-R10 is set up so that it may be set to R7=R8 and R9=R10. OP1-OP6 operate on the electrical potential difference of a VEE system, and VCC is not participating in formation of the panel driver voltage itself directly.

[0011] The power consumption at the time of using hereafter the power circuit shown in drawing 49 is described. The electrical potential difference applied to Y electrode at the time of un-choosing is VM, and the electrical potential differences applied to X electrode are Vx0-Vx4. The great portion of consumed electric current of the liquid crystal panel itself is a charge and discharge current which flows between X electrode and Y electrode in the condition of not choosing like the case of the one-line line sequential drive mentioned above. The power consumption by the charge and discharge current Ipn of a panel serves as IpnxVEE as GND=0V. however, it mentioned above — as — Vx0- the electrical-potential-difference difference of Vx4 and VM is quite small compared with the electrical-potential-difference difference between VEE-GND. Therefore, the rate of a deployment of Ipn is very low, and most only serves as heat loss in the path in which the inside of an operational amplifier is moved and it results to GND, and it becomes making an operational amplifier generate heat.

[0012] Furthermore, if the consumed electric current in the logic section of X driver etc. is set to IXD, the power consumption by this will serve as IXDxVEE instead of IXDxVCC. The part of IXDx (VEE-VCC) only serves as heat loss in the path in which the inside of an operational amplifier is too moved and it results to GND, and has become making an operational amplifier generate heat. According to two or more line coincidence sorting by selection, operating voltage width of face of X driver can be made small, but with this background technique, this advantage is not utilizable for power consumption reduction at all.

[0013] The power circuit of the liquid crystal display using 2 terminal mold nonlinear switching element as 3rd background technique is explained. As a power circuit which such a drive approach of a liquid crystal display is indicated by JP,5-34655,B, and is used in this case, there are some which were indicated by JP,5-46954,B and USP5,101,116. Hereafter, actuation and the configuration of this power

circuit are explained using drawing 50 (the driver voltage wave indicated by Fig.1A of USP5,101,116 is posted), and drawing 51 (the circuit indicated by this Fig.2B is posted). In drawing 50 , TPy (y= 1, 2, —, n) is a voltage waveform which drives Y electrode, and the non-choosing electrical potential difference after the selection electrical potential difference of a negative side and VM+ chose the selection electrical potential difference by the side of forward as for VD2 and VS2 chooses VD2, and VM− are the non-choosing electrical potential differences after choosing VS2. VD2−VS2 is about 40v, and the relation of VD2−VM+=VM—VS2 is realized mostly. That is, VC, then VD2 and VS2 are almost symmetrical mutually to VC in the central electrical potential difference of VD2 and VS2, and VM+ and VM− are also almost symmetrical mutually to VC.

[0014] VM+—VM− is quite small compared with VD2−VS2. Moreover, in the MLS drive mentioned above, both selection electrical potential differences of a forward side and a negative side are always need. On the other hand, in the liquid crystal display using 2 terminal mold nonlinear switching element, a selection electrical potential difference required at a certain time is only one side of VD2 or VS2, and both selection electrical potential differences are not needed in the same timing. Drawing 51 is the example of the circuit devised paying attention to this point so that pressure−proofing of Y driver could be managed with the abbreviation one half of VD2−VS2. VD2 makes ON and a transistor 252 turn off a transistor 250 to required timing. Thereby, VD (t) turns into VD2 which is an electrical potential difference higher than VM+, and VS (t) turns into VS1 which is an electrical potential difference higher than VS2 by capacity coupling. VS2 makes ON and a transistor 250 turn off a transistor 252 to required timing. Thereby, VS (t) turns into VS2 which is an electrical potential difference lower than VM−, and VD (t) turns into VD1 which is an electrical potential difference lower than VD2 by capacity coupling. When a selection electrical potential difference should give either a forward side or a negative side in the same timing, it is possible to finish pressure−proofing of Y driver in the abbreviation one half of VD2−VS2 by shaking the supply voltage applied to Y driver in this way. The drive method which shakes supply voltage in this way is shaken hereafter, and it expresses a power−source method. Current is in use in the liquid crystal panel for which this shaking power−source method used 2 terminal mold nonlinear switching element.

[0015] Although there is the advantage in which, as for a shaking power−source method, pressure−proofing of Y driver can be managed with the abbreviation one half of VD2−VS2 as mentioned above, there is a fault of making the power consumption of a liquid crystal display increase extremely. In order to carry out the charge and discharge of one of the causes which power consumption increases by the electrical−potential−difference width of face by which all the capacity that is parasitic on Y driver is shaken, it is for a current to flow in short within Y driver in the timing shaken. Another cause is because the power consumption of the power circuit itself is large, and is for there to be no good method of cutting down the power consumption of the power circuit itself.

[0016] When summarizing the above, there were the following troubles in the power circuit of a configuration like drawing 48 and drawing 49 .

[0017] (1) The invalid power consumption at the time of supplying the charge and discharge current of a panel is large.

[0018] (2) Since the consumed electric current in the logic section of X driver is also supplied from VEE of the high voltage, power consumption increases further.

[0019] (3) In order to use VEE of the high voltage as a power source of an operational amplifier, the power consumption by the idling current of the operational amplifier which flows from VEE regularly to GND is large.

[0020] (4) As an operational amplifier used for a power circuit, the low power quantity proof−pressure operational amplifier of an expensive rank must be used.

[0021] Moreover, power consumption cannot be reduced in the power circuit and drive method of the configuration of drawing 51 .

[0022] This invention solves the above technical problems and the place made into the purpose is to offer a cheap power circuit, a liquid crystal display, and electronic equipment with a low power.

[0023]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device - the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on the clock generated with the pulse-like clock including the pulse generated periodically, and supplies directly either [said] the 1st - the Nth potential through an adjustment means, It is characterized by including a means to stop charge of the pumping capacitor which said charge pump circuit contains, and charge of the backup capacitor by the pumping capacitor during the nascent state of said pulse of said pulse-like clock.

[0024] According to this invention, during the pulse nascent state of a pulse-like clock, charge of a pumping capacitor and a backup capacitor is suspended and, thereby, the recess of the charge in transition timing is prevented. In addition, as a pulse-like clock, the latch pulse used for a driver IC is the optimal.

[0025] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device - the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly said 1st potential by the side of high potential, or said Nth potential by the side of low voltage through an adjustment means, Charge pump actuation which charges a backup capacitor by turns by two or more pumping capacitors is performed based on a given clock. It is characterized by including the charge pump circuit which supplies directly the Ith potential in said 1st [the] - the Nth potential (1<I<N) through an adjustment means.

[0026] According to this invention, since a backup capacitor is charged by turns by two or more pumping capacitors, the output capacity of a charge pump circuit can be heightened. Generally the consumed electric current which must be supplied especially can improve a display property etc. effectively by generating the Ith potential of many middle potentials in the high charge pump circuit of this output capacity.

[0027] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device - the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly either [said] the 1st - the Nth potential through an adjustment means, It is characterized by including a means to make charge of the pumping capacitor which said charge pump circuit contains, and charge of the backup capacitor by the pumping capacitor perform for every 1 horizontal-scanning period in the drive of said display device.

[0028] According to this invention, charge pump actuation can be made to complete for every 1 level period, and, thereby, generating of display nonuniformity etc. can be prevented effectively.

[0029] Moreover, it is characterized by this invention performing charge pump actuation to which said charge pump circuit charges a backup capacitor by turns for every 1 level period by two or more pumping capacitors.

[0030] Thus, by charging a backup capacitor by turns for every 1 level period by two or more pumping capacitors, it becomes possible to make charge pump actuation complete for every 1 level period.

[0031] Moreover, this invention is characterized by including a means to suspend the given clock of said charge pump circuit.

[0032] According to this invention, display off control is attained only by the increment in very few element numbers, and the consumed electric current at the time of display OFF can be reduced to about 0.

[0033] Moreover, the liquid crystal display concerning this invention is characterized by including one of

the above-mentioned power circuits, the liquid crystal panel containing the liquid crystal layer driven with two or more data-line electrodes and two or more scanning-line electrodes, the data-line driver that drives said data-line electrode based on the potential supplied by said power circuit, and the scanning-line driver which drives said scanning-line electrode based on the potential supplied by said power circuit.

[0034] According to this invention, not only the power consumption of the power circuit itself but the power consumption of a liquid crystal display can be reduced, and the optimal liquid crystal display for a portable electronic device etc. can be offered.

[0035] Moreover, a means by which the liquid crystal display concerning this invention supplies the 1st input potential by the side of the high potential by which said power circuit is included in said input power electrical potential difference, and the 2nd input potential by the side of low voltage as either [said] the 1st – the Nth potential, Based on a given clock, perform charge pump actuation, and the charge pump circuit which supplies directly either [said] the 1st – the Nth potential through an adjustment means is included. It is characterized by using said 1st and 2nd input potential as supply voltage of one [at least] logic section of said data-line driver and a scanning-line driver.

[0036] According to this invention, while the 1st and 2nd input potential is used as either the 1st – the Nth potential, it is used also as supply voltage of the logic section of a data-line driver or a scanning-line driver. Thereby, it becomes unnecessary to give supply voltage independently for the logic sections, such as a data-line driver, and convenience of the user of equipment can be planned. Moreover, further low-power-ization of equipment can also be attained.

[0037] Moreover, it is characterized by this invention including the charge pump circuit which generates the potential in which said power circuit differs from said 1st and 2nd input potential by charge pump actuation based on a given clock, and supplies this generating potential as either [said] the 1st – the Nth potential.

[0038] When the supply voltage of the logic section differs from the potential difference of the Gth and Jth potential (1<G, J<N) used for a liquid crystal drive, for example according to this invention, it becomes possible to adjust so that these may become the same by the charge pump circuit. Thereby, it becomes easier to use the 1st and 2nd input potential as supply voltage of the logic section of a driver.

[0039] Moreover, it is characterized by including the charge pump circuit to which the liquid crystal display concerning this invention performs charge pump actuation, and supplies directly either [said] the 1st – the Nth potential through an adjustment means based on the clock by which said power circuit was generated with the latch pulse for said data-line drivers, or the shift clock for said scanning-line drivers.

[0040] A latch pulse and a shift clock are clocks of the shape of a pulse including the pulse generated periodically, and are the optimal as what generates the clock of a charge pump circuit. Therefore, by using these, it is compatible in maintenance of the display quality of a liquid crystal display, and a low power.

[0041] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device – the Nth (N>=4) potential. A means to supply the 1st input potential by the side of the high potential contained in said input power electrical potential difference as the Gth (1<G<N) potential in said 1st [the] – the Nth potential, A means to supply the 2nd input potential by the side of the low voltage contained in said input power electrical potential difference as the Jth (1<J<N) potential in said 1st [the] – the Nth potential, The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly said 1st potential by the side of high potential through an adjustment means, Charge pump actuation is performed based on a given clock, and it is characterized by including the charge pump circuit which supplies directly said Nth potential by the side of low voltage through an adjustment means.

[0042] When driving display devices, such as liquid crystal, generally there is little consumed electric

current which must be supplied with the 1st potential by the side of high potential and the Nth potential by the side of low voltage, and there is much consumed electric current which must be supplied with the Gth potential which is middle potential, and the Jth potential. And according to this invention, the 1st and Nth potential is supplied by the efficient charge pump circuit although output capacity is low, and the Gth and Jth potential is supplied by the high input power electrical potential difference of output capacity. Consequently, according to this invention, it becomes possible to be compatible in maintenance and low-power-izing of display quality, and the optimal power circuit for the liquid crystal display which aims at low-power-ization can be offered.
[0043] Moreover, this invention is characterized by supplying potentials other than said 1st, Gth, Jth, and Nth potential in said 1st [the] – the Nth potential with the charge pump circuit which carries out charge pump actuation based on a given clock, or a given operational amplifier.
[0044] Further low-power-ization can be attained if all potentials other than the 1st, Gth, Jth, and Nth potential are supplied by the charge pump circuit. On the other hand, by this invention, even if it uses the high operational amplifier of output capacity for supply of such potentials, since operating voltage of an operational amplifier can be made low, power consumption has the advantage of not getting worse so much.
[0045] Moreover, this invention is characterized by forming in said 1st input potential, said 2nd input potential, the middle point potential of this 1st and 2nd input potential, and a list at the symmetry to either of the middle point potentials of this generating potential at the time of generating potential which is different from this 1st and 2nd input potential in said 1st [the] – the Nth potential, and this 1st or 2nd input potential.
[0046] That is, according to this invention, the 1st – the Nth potential can be formed in the symmetry to the middle point potential of the symmetry or generating potential, and the 1st or 2nd input potential to the middle point potential of the symmetry or the 1st and 2nd input potential to the symmetry or the 2nd input potential to the 1st input potential.
[0047] Moreover, this invention generates this 1st and 2nd input potential and different potential based on either of said 1st and 2nd input potentials, and is characterized by making this generating potential into either of said Gth and Jth potential.
[0048] For example, compared with the potential difference of the 1st and 2nd input potential, the case where the potential difference of the Gth and Jth potential needed is large is considered. In this case, according to this invention, the Gth and Jth potential with the desired potential difference can be obtained, for example from the 1st input potential by generating higher potential. Thereby, low-battery-ization of a logic electrical potential difference etc. is attained.
[0049] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device – the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation of a pressure up K times (K>=2) based on a given clock, and supplies directly either [said] the 1st – the Nth potential through an adjustment means, Based on a given clock, L/M twice (however, L/M is not integer) pressure lowering or charge pump actuation of a M/L time pressure up is performed, and it is characterized by including the charge pump circuit which supplies directly either [said] the 1st – the Nth potential through an adjustment means.
[0050] According to this invention, a power circuit where a booster circuit and a 1/3 time pressure-lowering circuit are intermingled 6 times, for example is realizable. It enables this to supply the various electrical-potential-difference groups needed for the drive of a display device with a low power.
[0051] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device – the Nth (N>=4) potential. Based on a given clock, a pressure up, L/M twice (however, L/M is not integer) pressure lowering, or charge pump actuation of a M/L time pressure up is performed K times (K>=2). It is characterized by including the charge pump circuit which supplies directly either [said] the 1st – the Nth potential through an

adjustment means, and a means to change the pressure-up scale factor or pressure-lowering scale factor of said charge pump circuit.
[0052] According to this invention, it becomes possible to be able to change the scale factor of the pressure up or pressure lowering which a charge pump circuit performs, for example, to change a booster circuit into a booster circuit 5 times 6 times etc. For example, it becomes possible to form various needed driver voltage groups by changing a pressure-up scale factor etc. according to the value of the property of a display device, and an input power electrical potential difference. In addition, as for modification of a pressure up and a pressure-lowering scale factor, it is desirable to enable it to carry out even if it uses an external terminal etc.
[0053] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device - the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly said 1st potential by the side of high potential, or said Nth potential by the side of low voltage through an adjustment means, It is characterized by including a means to suspend supply of said 1st potential by the given period after the injection of said input power electrical potential difference, and said charge pump circuit, or said Nth potential.
[0054] According to this invention, after a given period passes after the injection of an input power electrical potential difference and a control circuit etc. operates normally, it becomes possible to make supply of the 1st or Nth potential start. Thereby, normal starting of a system becomes possible.
[0055] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device - the Nth (N>=4) potential. A means to supply the 1st input potential by the side of the high potential contained in said input power electrical potential difference as the Gth (1<G<N) potential in said 1st [the] - the Nth potential, A means to supply the 2nd input potential by the side of the low voltage contained in said input power electrical potential difference as the Jth (1<J<N) potential in said 1st [the] - the Nth potential, A means to be included in said input power electrical potential difference, and to supply the 3rd input potential by the side of high potential or low voltage rather than said 1st and 2nd input potential as said 1st potential by the side of high potential, or said Nth potential by the side of low voltage, The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly either of said 1st and Nth potential through an adjustment means, Charge pump actuation is performed based on a given clock. Rather than said Gth and Jth potential the Fth potential by the side of high potential or low voltage (1<F<N) It is characterized by supplying potentials other than said 1st, Fth, Gth, Jth, and Nth potential in said 1st [the] - the Nth potential including the charge pump circuit directly supplied through an adjustment means by the charge pump circuit which carries out charge pump actuation based on a given clock.
[0056] According to this invention, supply of the 1st - the Nth potential is attained with the circuit and the means of having the output capacity corresponding to the consumed electric current needed, and it can be compatible in maintenance and low-power-izing of display quality.
[0057] Moreover, this invention is a power circuit which supplies the 1st for an input power electrical potential difference being given and driving a display device - the Nth (N>=4) potential. The charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly either [said] the 1st - the Nth potential through an adjustment means, When at least one of the inputs of the supply interruption of said input power electrical potential difference, the supply interruption of said given clock, or a display off control signal is made, it is characterized by including a means to make the residual charge of a circuit part with which an electrical potential difference is supplied by at least one side of said 1st and Nth potential discharge.
[0058] According to this invention, the situation of the high voltage continuing being impressed to a display device is prevented, and improvement in dependability etc. can be aimed at.

[0059] Moreover, the electronic equipment concerning this invention is characterized by including said liquid crystal display.
[0060] According to this invention, low-power-ization of not only a liquid crystal display but the electronic equipment containing this can be attained. It enables this to prolong the battery life of electronic equipment, such as portable information machines and equipment, etc.
[0061]
[Embodiment of the Invention] Hereafter, the example of this invention is explained based on a drawing. In addition, unless it describes especially, explanation is advanced, using potential of GND as 0V for convenience.
[0062] [Example 1] The block diagram of the power circuit of an example 1 is shown in drawing 1 . This power circuit has the function to generate the same output voltage as the power circuit of drawing 49 .
[0063] The input power electrical potential differences of this power circuit are only Vcc (the 1st input potential) and GND (the 2nd input potential), and serve as a single power supply input. Moreover, the latch pulse LP which consists of the pulse generated for every horizontal scanning period is inputted. The clock formation circuit 1 forms some clock signals required for a charge pump circuit with which timing differs based on LP, and is using Vcc and GND as the power source. The negative 6 times as many direction [as this] booster circuit 2 generates the pressure up electrical potential difference [GND] VEE on the basis of Vcc by charge pump actuation 6 times in the negative direction. VEE is set to -16.5V when Vcc is 3.3V. The contrast equalization circuit 3 generates the selection electrical potential difference VL used as the optimal contrast based on VEE. This VL serves as a negative side selection electrical potential difference of Y electrode. The 2 double booster circuit 4 generates the selection electrical potential difference VH by the side of 2-double-pressure-up-forward [on the basis of VL] in GND by charge pump actuation. The negative direction 2 double booster circuit 5 is a 2 double pressure up electrical potential difference [GND / direction / negative] on the basis of Vcc. - V3 is generated by charge pump actuation. 1 / 2 pressure-lowering circuits 6 and 7 are V2 which is the electrical potential difference which divided between Vcc-GND into two equally, and the electrical potential difference which divided between GND- (- V3) into two equally. - V2 is generated by charge pump actuation. GND is used for the central potential VC as it is. Moreover, GND is received. - Vcc is used for V3 and V3 which is symmetrical potential as it is. The electrical potential difference which drives a liquid crystal panel above has been formed. In this power circuit, the electrical potential differences VH, V3, V2, and VC outputted, -V2, -V3, and VL serve as symmetry to GND (the 2nd input potential). In addition, from VL, only Vcc forms a high electrical potential difference and a circuit 8 supplies this for it as a logic electrical potential difference VDDy of Y driver. Since the VDDy itself is not directly added to a panel, it is outside the object of the symmetric property of an electrical potential difference.
[0064] This example explained above has the description on the following configurations.
[0065] (1) Use the 1st input potential Vcc by the side of the high potential contained in an input power electrical potential difference, and the 2nd input potential GND by the side of low voltage as it is in this example as the Gth potential V3 in the 1st - the Nth potential (N>=4), and the Jth potential VC. Moreover, charge pump actuation is performed based on a given clock, and the 2 double booster circuit 4 and the negative 6 times as many direction [as this] booster circuit 2 which supply directly the 1st potential VH by the side of high potential and the Nth potential VL by the side of low voltage through an adjustment means (contrast equalization circuit 3) are included.
[0066] As explained in the background technique, that to which the consumed electric current of the liquid crystal panel itself flows between the non-choosing electrical potential difference VC of Y electrode, the driver voltages V3 and V2 of X electrode, -V2, and -V3 is most. For example, in the case of 1/240 duty, it is because all of the remaining 236 lines are in the condition of not choosing, to Y electrode of a selection condition being only four lines. This example has connected the high input

power electrical potential differences Vcc and GND of output capacity to the Gth potential V3 and the Jth potential VC which are middle potential while supplying the 1st potential VH and the Nth potential VL in an efficient charge pump circuit paying attention to this point, although output capacity (current serviceability) is low. By doing in this way, it is compatible in maintenance and low-power-izing of display quality. On the other hand, since the power circuit of drawing 49 has the composition that all currents flow between the 1st potential VEE and the Nth potential GND, the output capacity of the circuit which forms VEE must be high. Therefore, it is impossible to supply VEE in a charge pump circuit, and it is hardly incompatible in maintenance and low-power-izing of display quality.

[0067] (2) Supply potentials V2 other than said 1st, Gth, Jth, and Nth potential in the 1st – the Nth potential, –V2, and –V3 in this example by 1 / 2 pressure-lowering circuits 6 and 7, and the negative direction 2 double booster circuit 5 which carry out charge pump actuation based on a given clock. Thus, further low-power-ization can be attained by supplying V2, –V2, and –V3 by the charge pump circuit. And since a clock required for charge pump actuation is sharable between charge pump circuits according to this example, control is easy and increase of a circuit scale can also be suppressed to the minimum.

[0068] In addition, the block diagram in the case of supplying V2 and –V2 to drawing 2 with operational amplifiers OP1 and OP2 is shown. Bleeder resistance for R1 and R3 to carry out voltage division of between V3 and VC (GND), and R2 and R4 are the bleeder resistance for carrying out voltage division of between VC and V–3. Moreover, OP1 and OP2 are the operational amplifiers for outputting the electrical potential difference divided by bleeder resistance by low impedance. Moreover, R11 and R12 are resistance for cutting down the power consumption both which restricts the output current of OP1 and OP2, and attains stabilization of operation, and it is a smoothing capacitor for suppressing fluctuation of C1–C 4V2, and –V2. OP1 uses V3 and VC as a power source, and OP2 operates considering VC and –V3 as a power source. C4 may be arranged between VC and V–3 between C 1V3 and VC. Thus, even if it supplies V2 and –V2 with operational amplifiers OP1 and OP2, since OP1 and OP2 operate with small supply voltage unlike the power circuit of drawing 4949 , they can stop the power consumption of this part in tolerance.

[0069] (3) Moreover, this example performs charge pump actuation of a pressure up K times (K>=2) based on a given clock. The negative 6 times as many direction [as this] booster circuit 2 which supplies either the 1st – the Nth potential through an adjustment means (contrast equalization circuit 3) directly, the 2 double booster circuit 4, and the negative direction 2 double booster circuit 5, Based on a given clock, L/M twice (however, L/M is not integer) pressure lowering or M/L twice as many charge pump actuation as this is performed, and 1 / 2 pressure-lowering circuits 6 and 7 which supply either the 1st – the Nth potential through an adjustment means directly are included. Thus, the charge pump circuit which performs a pressure up K times, and the charge pump circuit which performs L/M twice pressure lowering etc. are made intermingled in this example. This becomes possible from single input power (Vcc, GND) to supply various electrical potential differences with a low power.

[0070] Next, the contrast equalization circuit 3 is explained using drawing 3 . The contrast equalization circuit 3 contains the fixed resistance Rfix and the variable resistance Rvol and the bipolar transistor Tr which were inserted by the series connection between GND–VEE, and Capacitor CVL. In the liquid crystal display driven in the power circuit of this example, since the current which flows output voltage VL is small, the base current of Tr is also small and ends. Consequently, by 500Kohm–1M omega and high resistance, Rfix and Rvol are good and can hold down the power consumption by this resistance to 0.2mW – about 0.4mW.

[0071] In addition, although the contrast equalization circuit 3 was established only in the VL side in drawing 1 , it may prepare only in the VH side or you may prepare in both by the side of VH and VL. In drawing 1 , the contrast equalization circuit 3 is established only in one side, and the 2 double booster circuit 4 is generating VH based on the electrical potential difference VL obtained in the contrast

equalization circuit 3. With this configuration, there is an advantage that VH can also be automatically adjusted by adjusting VL by the contrast equalization circuit 3. On the other hand, according to the configuration which establishes the contrast equalization circuit 3 in the both sides of VH and VL, there is an advantage that VH and VL can be adjusted independently. Nonlinear switching elements, such as MIM, have the thing property that the sink easy of a current changes with directions which impress an electrical potential difference. therefore — the liquid crystal display using MIM etc. — |VH| — |VL| — receiving — 0.5 — it may be desirable to make it low about V Therefore, in such a case, it is desirable to establish a contrast equalization circuit in both by the side of VH and VL. What is necessary is to include diode etc. in the contrast equalization circuit by the side of VH, and just to specifically lower the pressure of VH using the forward voltage of this diode.

[0072] Moreover, what is necessary is to have formed 1 / 2 pressure-lowering circuits 6 and 7 in drawing 1 , in order to obtain the electrical potential difference of 7 level, but just to omit 1 / 2 pressure-lowering circuits 6 and 7, when a desired electrical potential difference is 5 level.

[0073] According to this example of the above configuration, low-power-ization of the liquid crystal display driven with four-line coincidence sorting by selection is attained for the reason explained below.

[0074] The first reason is that the power consumption by the charge and discharge current of a panel decreases even on an extreme target. The charge and discharge current which occupies most panel currents, i.e., the charge and discharge current which flows between X electrode and Y electrode in the condition of not choosing, is considered. The charge and discharge current which flows between the electrical potential difference V3 of X electrode, -V3, V2, -V2, and the electrical potential difference VC of Y electrode is respectively set to IP3, IM3, IP2, and IM2. Then, the power consumption by IP3 serves as VccxIP3. Moreover, it becomes VccxIM3 mostly and the power consumption by IM3 since the charge pump circuit is very efficient, and the power consumption by IP2 and IM2 serve as xVccxIP2 and x(1/2) VccxIM2 mostly (1/2) respectively. On the other hand, in the example of a background of drawing 49 , if the high voltage is set to VEE, the power consumption by each [these] current will serve as VEExIP3, VEExIM3, VEExIP2, and VEExIM2. Since VEE is about 25V and Vcc is about 3.3V, the power consumption by IP3 and IM3 becomes 1/7 or less [of the example of a background], and 1/14 or less is the power consumption by IP2 and IM2.

[0075] Next, the charge and discharge current which flows between X electrode and Y electrode of a selection condition is considered. The charge and discharge current which flows between the electrical potential differences VH and VL of Y electrode and X electrode is respectively set to IVHIVL. Then, too, the power consumption by IVH and IVL serves as 5xVccxIVH and 5xVccxIVL from the efficient nature of a charge pump circuit mostly respectively, and it becomes small rather than the power consumption of the example of a background.

[0076] The second reason is that it operates at high speed and the power consumption in the logic section of large X driver of the consumed electric current decreases. As mentioned above, since the consumed electric current in the logic section of X driver is supplied from the high voltage VEE, power consumption serves as the VEEx consumed electric current in the power circuit of the example of a background. On the other hand, in this example, power consumption serves as the Vccx consumed electric current, and becomes 1/7 or less [of the example of a background].

[0077] The third reason is that the power consumption of the booster circuit which forms the high voltage VEE is small. Generally, if the booster circuit of a charge pump type has small pressure-up capacity and takes out a big current, output voltage will decline. In the booster circuit of a charge pump type, it is deficiency in performance forming VEE in the liquid crystal display driven in the power circuit of the example of a background, since the current of a high-voltage system is large. Therefore, in the example of a background, the DC-DC converter of the switching regulator method which rectifies the high voltage generated when intermittent in the current passed in a coil, and forms the high voltage VEE is used. The effectiveness of the DC-DC converter of a switching regulator method is the thing of 5V

input, and is usually very as low as about 60% in the thing of 3.3V input about 80%. For this reason, when it includes to the booster circuit which forms VEE, the power consumption of the liquid crystal display driven in the power circuit of the example of a background is very large. On the other hand, the liquid crystal display driven in the power circuit of this example has the small current of a high-voltage system. Therefore, the high voltage VEE can be supplied in an efficient charge pump type booster circuit, although output capacity is small, and the power consumption included to the booster circuit which forms VEE can be reduced greatly.

[0078] The above is the reason whose low-power-ization of a liquid crystal display is attained by the power circuit of this example. When the liquid crystal display of 2 screen drives whose number of dots is 640x480 and whose dot pitch is 0.2mm was actually driven in the power circuit of the method of drawing 1 R> 1, typical power consumption was a value as expected [of about 12mW].

[0079] In addition, when IC-izing the power circuit of this example, as for formation of VL, it is possible to also make the regulator of the operational amplifier format instead of the method which carries out external [of the circuit by the bipolar transistor mentioned above] build in IC. Moreover, in order to lower pressure-proofing of IC, it is also a practical means to make external the transistor which switches VH-GND among the components which constitute the 2 double booster circuit 4 for VH formation, and to summarize except [its] for one chip.

[0080] In the power circuit of this example, since most of the configurations are formed in the charge pump circuit, the impression which needs many capacitors is given. However, it is possible to omit in fact some backup capacitors contained in a charge pump circuit, or to be a thing with a small capacity value of about 0.1 micro F, and to finish. This is considered for the capacity which the liquid crystal panel itself has to work as a backup capacitor.

[0081] [Example 2] An example 2 is an example about the clock formation circuit 1 of drawing 1 , and shows the timing chart for explaining an example of the configuration to drawing 4 , and explaining the actuation to drawing 5 . This whole circuit operates by the Vcc-GND system. Moreover, the latch pulse LP which includes the pulse generated in every horizontal scanning period (1H) as a basic clock signal is used. A /Q output writes in, it connects with data input D, and, thereby, d-type-flip-flop DF carries out toggle actuation by the rising edge of LP. NOR circuits Nor1 and Nor2 are for forming the clock signals A and B of two phases, and inverter circuits Inv1, Inv2, and Inv3 are respectively for forming the signal/A of the opposition of A, B, and /Doff, /B, and Doff.

[0082] (1) Charge pump actuation is made to perform in a charge pump circuit (negative 6 times as many direction [as this] booster circuit 2 grade of drawing 1) in pulse-like clock this example based on the clock generated with the pulse-like clock LP including the pulse (P1 of drawing 5 , P2 grade) generated periodically. And charge of the pumping capacitor which a charge pump circuit contains, and charge of the backup capacitor by the pumping capacitor are stopped during the nascent state of the pulse of the pulse-like clock LP. That is, he is trying, as for between the nascent states of the pulse of LP (period when LP is high-level), to set Signal A and Signal B to a low level, as shown in Tp of drawing 5 . If Signals A and B are set to a low level, all the switch groups (transistor group) that form a charge pump circuit become off, and, thereby, can prevent the recess of the charge in transition timing.

[0083] However, since the time amount which charges a pumping capacitor and a backup capacitor conversely will become short if the off time amount of the switch group in this transition timing is too long (if the period of Tp is too long), a required electrical potential difference is no longer obtained. Since 100ns - about 300ns and a period are usually the pulse-like clocks which are dozens of microseconds - about 100 microseconds, pulse width of LP is convenient as a basic clock of this circuit. Moreover, since the charge and discharge of a panel happen 1 horizontal-scanning (1H) period, charging the driver voltage of a panel 1H period using LP suits **. It becomes that it is [a circuit] easier to divert the latch pulse inputted into a driver IC also to the basic clock of this power circuit and is desirable although it is also possible not to consider LP as an input but to carry out bulk generation of

the basic clock in CR oscillator circuit etc.

[0084] In addition, not only LP that is a latch pulse for X drivers but the shift clock YSCL for for example, Y drivers etc. may be used for the pulse-like clock used by this example. Moreover, what is necessary is just to make the period Tp which makes a switch group turn off using a delay circuit etc., in not using a pulse-like clock.

[0085] (2) A display off control signal / Doff makes Signal A and Signal B a low level in between at a low level, and he is trying for actuation of a charge pump circuit to stop in the stop function and this example of a clock. That is, the function to suspend the clock given to a power circuit in a charge pump circuit is given. By adding this function, power consumption of the power circuit at the time of display off control is made to about 0. Moreover, since the output of a selection electrical potential difference stops to coincidence, even if it uses what does not have a display off control function in Y driver, it becomes possible to give a display off control function as the whole liquid crystal display. In addition, in consideration of the test ease when IC-izing a power circuit, by applying reset to DF, generating of a clock was suspended and actuation of a charge pump circuit is suspended in the example of drawing 4 . However, even if it uses the approach of inputting LP and /Doff into a given AND circuit, and using the acquired signal as a new basic clock, it is possible to suspend actuation of a charge pump circuit.

[0086] [Example 3] An example 3 is an example about the negative 6 times as many direction [as this] booster circuit 2 of drawing 1 , and the charge pump circuit of 2 double booster circuit 4 grade.

[0087] (1) Fundamental concept drawing 6 is the basic conceptual diagram of a charge pump circuit most. While SWa and SWb are interlock switches and one side has fallen on the A side in drawing 6 , another side has also fallen on the A side. Moreover, although the mechanical switch expressed SWa and SWb in drawing 6 , the two usual transistor of the MOS transistor which controls the flow and cutoff by the side of A, and the MOS transistor which controls the flow and cutoff by the side of B can constitute Switches SWa and SWb in fact.

[0088] While SWaSWb has changed to the A side, the pumping capacitor Cp is charged on the electrical potential difference of Vb-Va. Subsequently, if SWaSWb changes to the B side, the charge charged by Cp will be transmitted to the backup capacitor Cb. By repeating this switching operation, the electrical potential difference which has joined Cb, i.e., the electrical potential difference between Ve-Vd, approaches a value almost equal to the electrical potential difference between Vb-Va. In being the fixed electrical potential difference with Vd at this time, an electrical potential difference only with Vb-Va higher than Vd occurs in Ve. On the contrary, in being the fixed electrical potential difference with Ve, an electrical potential difference only with Vb-Va lower than Ve occurs in Vd. The above is basic actuation of a charge pump circuit. Next, by where Va, Vb, Vd, and Ve are connected, this circuit functions as a booster circuit, or functions as a pressure-lowering circuit so that it may state.

[0089] (2) 2 double pressure-up drawing 7 is what connected Vd to Vb in drawing 6 , and serves as a conceptual diagram of the charge pump circuit for 2 double pressure ups. That is, since it becomes Ve-Vd=Ve-Vb=Vb-Va for the reason mentioned above because SWa and SWb repeat interlocking switching operation, Ve-Va=(Ve-Vb)+(Vb-Va)=2x (Vb-Va) is materialized. That is, if Va is made into the reference level (0V) of potential, it will be set to Ve=2xVb, and Ve serves as an electrical potential difference which carried out 2 double pressure up of the Vb.

[0090] (3) Negative direction 2 double pressure-up drawing 8 is what connected Ve to Va in drawing 6 , and serves as a conceptual diagram of the charge pump circuit for negative direction 2 double pressure ups. Since it becomes Ve-Vd=Va-Vd=Vb-Va because SWa and SWb repeat interlocking switching operation, Vb-Vd=(Vb-Va)+(Va-Vd)=2x (Vb-Va) is materialized. That is, if Vb is made into the reference level (0V) of potential, it will be set to Vd=2xVa, and Vd serves as an electrical potential difference which carried out 2 double pressure up of the Va in the negative direction.

[0091] (4) 1 / 2 pressure-lowering drawing 9 changes input voltage into Vb-Vd from Vb-Va in drawing 8 , and is the conceptual diagram of 1 / charge pump circuit for 2 pressure lowering. Ve is output voltage

and the current which the load connected with Ve consumes is supplied from the backup capacitor Cb. First, when SWaSWb has flowed the B side, since Cp and Cb become parallel connection, the electrical potential difference which has joined this Cp and Cb is equal [Cb]. Next, if SWa and SWb cut and change to the A side, Cp used as series connection and Cb will serve as the form where it enters between input voltage Vb–Vd, and the electrical potential difference which joins Cp and Cb will serve as half [of input voltage]. Subsequently, if SWaSWb cuts and changes to the B side again, since Cp and Cb become parallel connection, the electrical potential difference on which the charge currently stored in Cp joins the electrical potential difference which is supplied to Cb and joins Cp, and Cb will become equal. Therefore, if the charge which can be stored in Cp and Cb is fully large compared with the charge away held by the load current of Ve, in Ve, the output voltage near one half of input voltage will occur because SWa and SWb repeat interlocking switching operation.

[0092] (5) Negative 6 times as many direction [as this] pressure-up drawing 10 is the conceptual diagram showing an example of the charge pump circuit for the negative 6 times as many direction [as this] pressure ups, and drawing 11 (A) and drawing 11 (B) are connection relation Figs. when SWa1–SWa3, and SWb1–SWb3 have changed to the A and B side respectively. SWa1–SWa3, and SWb1–SWb3 are interlock switches, and, as for Cp1–Cp3, a pumping capacitor, and Cb1 and Cb23 are backup capacitors.

[0093] By the same actuation as the negative direction 2 double booster circuit mentioned above, –2x (Vcc–GND) which is the electrical potential difference which carried out 2 double pressure up of the GND in the negative direction on the basis of Vcc occurs in –V3B. Since Cp2 and Cp3 become parallel connection as shown in drawing 11 (A) when all switches have changed to the A side, Cp2 and Cp3 will be respectively charged on the electrical potential difference of about 2 x (Vcc–GND).

[0094] Next, if all switches cut and change to the B side, as shown in drawing 1111 (B), parallel connection of the Cp2 and Cp3 by which series connection was carried out will be carried out to Cb23. Cp2 and Cp3 are charged by 2x (Vcc–GND) as mentioned above. Therefore, between –V3B and VEE, the electrical potential difference of 4x (Vcc–GND) occurs, and Cb23 is charged on this electrical potential difference. From the above reason, in VEE, the 6 time pressure up electrical potential difference on the basis of Vcc, i.e., Vcc–6x, (Vcc–GND) generates GND in the negative direction because all switches repeat interlocking switching operation. For example, in the case of Vcc=3V, the electrical potential difference of –15V occurs at –V3B at –3V and VEE.

[0095] Drawing 12 is the conceptual diagram showing other examples of the charge pump circuit for the negative 6 times as many direction [as this] pressure ups, and drawing 13 (A) and drawing 13 (B) are connection relation Figs. when SWa1–SWa3, and SWb1 and SWb23 have changed to the A and B side respectively. As for Cp1–Cp3, a pumping capacitor, and Cb1–Cb3 are backup capacitors.

[0096] In –V3B, –2x (Vcc–GND) which is a 2 double pressure up electrical potential difference on the basis of Vcc generates GND in the negative direction like the circuit of drawing 10 . When all switches have changed to the A side, as shown in drawing 13 (A), Cp2 is charged on the electrical potential difference of about 2 x (Vcc–GND). Moreover, the circuit which consists of Cp2, Cb2, SWb23, and SWa2 as shown in drawing 12 is a negative direction 2 double booster circuit as well as the circuit which consists of Cp1, Cb1, SWb1, and SWa1. Therefore, it charges on the electrical potential difference of 2x (Vcc–GND), and the electrical potential difference of –4x (Vcc–GND) also generates Cb2 in VEM. Cp3 will be charged on the electrical potential difference of 4x (Vcc–GND) by this.

[0097] Next, if all switches change to the B side, as shown in drawing 1313 (B), it will become the connection relation in which CP3 is inserted between –V3B and VEE. – Electrical potential difference of V3B – It is 2x (Vcc–GND) and Cp3 is charged on the electrical potential difference of 4x (Vcc–GND). Therefore, in VEE, the 6 time pressure up electrical potential difference on the basis of Vcc, i.e., the electrical potential difference of Vcc–6x (Vcc–GND), generates GND in the negative direction after all.

[0098] Since the circuit of drawing 10 has unnecessary VEM which is the electrical potential difference

by which the middle of −V3B and VEE was stabilized unlike the circuit of drawing 12, it has the advantage that there may be few one required capacitors than the circuit of drawing 12. On the other hand, since the switch which leads to + electrode of Cp2 and Cp3 is shared, the circuit of drawing 12 R> 2 has the advantage that there may be few one required switches than the circuit of drawing 10 (it is two as a transistor count). Furthermore, there is also an advantage that drain pressure−proofing of a transistor may come to be lower than the circuit of drawing 10 by forming intermediate voltage VEM, and size of a transistor can be made small.

[0099] (6) 3 / 2 double pressure−up drawing 14 (A), and drawing 14 (B) are the conceptual diagrams of 3 / charge pump circuit for 2 double pressure ups. CpHCpL is a pumping capacitor and Cb is a backup capacitor. As shown in drawing 14 (A) and 14 (B), in this circuit, the condition that CpH, CpL, and Cb are series connection, and the condition that Cb, CpH, and CpL are parallel connection are repeated by turns. If the electrical potential difference which has joined CpHCpL is respectively expressed as VcpH and VcpL, since CpH and CpL are parallel connection by drawing 14 (B), it will become VcpH=VcpL. Moreover, when CpH and CpL become series connection between Vcc−GND like drawing 14 (A), one half of the electrical potential differences of Vcc are charged by CpH and CpL. Then, when it changes into the connection condition of drawing 14 (B), the charge currently stored in CpH and CpL is supplied to Cb. By repeating this actuation repeatedly, the electrical potential difference which approached one half of Vcc(s), consequently carried out the pressure up of the Vcc to output voltage 3/2 generates each electrical potential difference which has joined Cb, CpH, and CpL.

[0100] (7) Negative direction 3 / 2 double pressure−up drawing 15 (A), and drawing 15 (B) are the conceptual diagrams of negative direction 3 / charge pump circuit for 2 double pressure ups. Since the principle of operation is the same as that of the above−mentioned 3 / 2 double pressure up, detailed explanation is omitted. The above−mentioned 3 / 2 double pressure up can obtain pressure−up electrical−potential−difference−3/2xVcc of hard flow by repeating by turns the condition of drawing 15 (A) that the pumping capacitors CpH and CpL are the backup capacitor Cb and series connection, and the condition of drawing 15 (B) that Cb, and CpH and CpL are parallel connection, like the case of 3 / 2 double pressure up. Low−power−ization of a liquid crystal display is attained at the driver IC of a liquid crystal display by sometimes often needing the electrical potential difference of a negative side, and applying this circuit to such a liquid crystal display rather than a logic electrical potential difference and its logic electrical potential difference.

[0101] (8) 2/3 time pressure−lowering drawing 16 (A) and drawing 16 (B) are the conceptual diagrams of the charge pump circuit for 2/3 time pressure lowering. Also in this circuit, the condition of drawing 16 (A) that the pumping capacitors CpH and CpL are the backup capacitor Cb and series connection, and the condition of drawing 16 (B) that Cb, and CpH and CpL are parallel connection are repeated by turns. the time of the electrical potential difference which has joined Cb, CpH, and CpL becoming the same from becoming parallel connection in drawing 16 (B) altogether, and becoming series connection like drawing 16 (A) — Cb, and CpH and CpL — respectively — about [of Vcc] — one third of electrical potential differences are charged. By repeating this actuation repeatedly, about 1/approaches 3, consequently, as for each electrical potential difference which has joined Cb, CpH, and CpL, the electrical potential difference of Vcc on which the pressure was lowered generates an electrical potential difference only with low x (1/3) Vcc, i.e., Vcc, 2/3 time from Vcc in an output.

[0102] (9) Negative 2/3 time as many direction [as this] pressure−lowering drawing 17 (A) and drawing 17 (B) are the conceptual diagrams of the charge pump circuit for the negative 2/3 time as many direction [as this] pressure lowering. Since the principle of operation is the same as that of the above−mentioned 2/3 time pressure lowering, detailed explanation is omitted. In 2/3 time pressure lowering, pressure−lowering electrical−potential−difference−2/3xVcc of hard flow can be obtained by repeating by turns the condition of drawing 17 (A) that CpH and CpL are the backup capacitor Cb and series connection, and the condition of drawing 17 (B) that Cb, and CpH and CpL are parallel connection, like

the case of 2/3 time pressure lowering.

[0103] (10) The example at the time of constituting a part for the radical headquarters of the charge pump circuit for negative direction 2 double pressure ups shown in example drawing 18 of a charge pump circuit at drawing 8 from discrete part is shown (when it is discrete and being constituted). Vx is made into input voltage, Vy is made into output voltage, and it is referred to as Vx>0. Trp1 and Trp2 of a PMOS transistor turn on to timing T1 (refer to drawing 19), and the pumping capacitor Cp is charged on the electrical potential difference of Vx-GND. At this time, Trn1 and Trn2 of N-MOS transistor turn off. To the following timing T2, while making Trp1 and Trp2 turn off, Trn1 and Trn2 are made to turn on, and the charge charged by the pumping capacitor Cp is moved to the backup capacitor Cb. If the source electrode of Trn1 is connected to GND like drawing 18 , in an output Vy, Vx and a symmetrical electrical potential difference will occur to GND by repeating actuation of the above-mentioned timing T1 and T2 by turns.

[0104] The signal which goes into the gate of a transistor in drawing 18 / A1 / A2 and B, and B-2 are the signals of a phase and an electrical potential difference as shown in drawing 19 . When the level of these signals is not between VC and GND, the means which carries out the level shift of the signal is needed. The easy level shift approach in the case of using discrete part is an approach of using a coupling capacitor Cs and Diode D like drawing 20 (A) and drawing 20 (B). There should just be about 470pF of capacity of a coupling capacitor Cs. By connection of drawing 20 (A), the gate signal which are a signal/A, in phase, and this amplitude, and can turn on / turn off the PMOS transistor Trp / Ax can be obtained. Moreover, by connection of drawing 20 (B), it is Signal B, in phase, and this amplitude, and the gate signal Bx which can turn on / turn off the NMOS transistor Trn can be acquired. Rp is several M omega resistance and is serving to compensate the leakage current of diode and to stabilize the electrical potential difference of a gate signal.

[0105] The above described the case where a charge pump circuit was constituted using discrete part. On the other hand, what is necessary is just to adopt as the transistor configuration and level shift means of a charge pump circuit well-known configuration and means to have been more suitable for monolithic IC-ization, when monolithic-IC-izing a charge pump circuit.

[0106] (11) The example of a configuration of the charge pump circuit at the time of using diodes D1 and D2 instead of a transistor as a switching device is shown in the charge pump circuit diagram 21 using diode. V1 is the stable input voltage, an amplitude electrical potential difference is **** and Vx is the high clock of drive capacity. According to this circuit, about 0.6V, then output voltage V2=V1- (clock amplitude electrical potential difference **** - about 0.6 V) can be efficiently generated for the forward voltage of diode.

[0107] Next, actuation is explained using the timing chart of drawing 22 . In addition, in order to simplify explanation, forward voltage of diodes D1 and D2 is set to 0V. In Period Tc, it is Vx=Va, and since D1 is a forward bias, it is Vd=V1. Therefore, Capacitor Cp is charged on the electrical potential difference of V1-Va. If Period Td comes, the level of Vd will be pulled by Cp and only the **** which is a part for the voltage drop of Vx will fall. Thereby, a current flows by the root of V1 ->Cb->D2 ->Cp->Vx, and Cb is charged. Output voltage V2=V1-**** can be obtained by repeating the actuation in the above periods Tc and Td.

[0108] In addition, if two steps of circuits of drawing 21 are piled up as shown in drawing 23 , the electrical potential difference of V1-2x (**** - about 0.6 V) can be obtained as V3. If three steps lap similarly, the electrical potential difference of V1-3x (**** - about 0.6 V) can be obtained.

[0109] As mentioned above, various things, such as a thing not only using a thing but the diode using a transistor etc. as a charge pump circuit of this invention, are employable.

[0110] [Example 4] An example 4 is an example about the technique of enlarging output capacity (current serviceability) of a charge pump circuit. Although output capacity can be enlarged if on resistance of the transistor which forms a charge pump circuit is fundamentally made low and capacity

value of a capacitor is enlarged, to be based on other technique may be more efficient. Two or more pumping capacitors are prepared as that one technique, and the technique of charging a backup capacitor by turns by two or more of these pumping capacitors can be considered. The technique of adding the circuit which doubles the frequency of LP as the other technique, and carrying out charge actuation and pump actuation for every half period of LP is also possible. For example, it can set to drawing 1 . − V3 starts sag to a duplex according to the current consumed in the circuit part connected with −V3, and the current consumed in the circuit part connected with −V2. Therefore, as for the charge pump circuit which supplies −V3, it is desirable to enlarge output capacity by the above-mentioned various technique.

[0111] Two or more pumping capacitors Cp1 and Cp2 are formed in drawing 24 , and the example of a circuit which heightens output capacity is shown. The example at the time of constituting a circuit from discrete part is shown like drawing 18 also here.

[0112] Signal A / A, B/B is the signals formed by the clock formation circuit explained by drawing 4 , and Vx is input voltage. A sets a high-level period to T1, and B sets a high-level period to T2. Trn1, Trn2, Trp3, and Trp4 turn off the period of T1, and Trp1 and Trp2 turn on. Thereby, Cp1 is charged on an electrical potential difference Vx. Moreover, since Trn3 and Trn4 are turned on, the charge charged by last time Cp2 moves to Cb. Next, in the period of T2, Trp1, Trp2, Trn3, and Trn4 turn off, and Trp3 and Trp4 turn on. Thereby, Cp2 is charged on an electrical potential difference Vx. Moreover, Trn1 and Trn2 are turned on and accumulated and the charge charged by last time Cp1 moves from them to Cb. Thus, the smoothness of output voltage can realize the good large charge pump circuit of output capacity more by supplying a charge to Cb by turns by two charge pump capacitors Cp1 and Cp2.

[0113] In addition, the part shown in H of drawing 24 is a level shift means for forming a signal with an electrical potential difference and a phase required driving the gate of the transistor of Trp2, Trp4, Trn2, and Trn4 from Signals A/B. As for diode and Inv 3-6, an inverter, and Rf1 and Rf2 are [the coupling capacitor whose capacity of Cs1 and Cs2 is about 470pF, and D1 and D2] resistance of an about [1Kohm]. One hold circuit is formed by Inv3, and Inv4 and Rf1, and another hold circuit is formed by Inv5, and Inv6 and Rf2. If it is made connection like drawing 24 and the forward side power supply terminal of Inv 3-6 is connected to GND, since an electrical potential difference only with Vx lower than GND will occur in the negative side power supply terminal of Inv 3-6, the signal of an inphase/opposition is acquired from the output of Inv 3-6 with Signal A, and a signal/B and this amplitude. It is desirable to put in the about 0.1-micro F smoothing capacitor Cx between the power supply terminals of Inv 3-6. This level shift means has the advantage that the amplitude fall of a signal is smaller than the level shift means explained by drawing 20 (A) and drawing 20 (B).

[0114] Now, although two or more pumping capacitors are prepared in this example in order to raise output capacity, this technique has effectiveness also in improvement in display quality. For example, according to the technique using the latch pulse LP, as shown in drawing 25 (A), charge (charge actuation) of the pump capacitor Cp and charge (pump actuation) of the back-up capacitor Cb by Cp will be repeated by every 2 horizontal-scanning period (2H). If such a charge pump circuit of a configuration is used for the negative direction 2 double booster circuit 5 of drawing 1 , the display nonuniformity (deep 4line+-light four lines)-of the disk in a cycle of eight line may produce it. It is because the current with which the negative direction 2 double booster circuit 5 supplies the current consumed by both −V2 and −V3, and −V2 and −V3 are consumed compared with VH and VL is large. Then, the configuration which has two or more pumping capacitors as show the negative direction 2 double booster circuit 5 to drawing 24 , then generating of the above display nonuniformity can be prevented effectively. The reason is that charge of Cp1 or Cp2 and charge of Cb by Cp2, or charge of Cb by Cp1 will be performed for every 1 level period as shown in drawing 25 (B) if it does in this way.

[0115] In addition, what is necessary is just to charge the backup capacitor by charge of a pumping capacitor, and the pumping capacitor for every 1 level period at least, in order to prevent generating of

the above display nonuniformity. If charge pump actuation is performed as it follows, for example, is shown in drawing 25 (C) using a signal twice the frequency of the latch pulse LP, the above-mentioned display nonuniformity can be prevented.

[0116] [Example 5] An example 5 is an example about modification of the pressure-up scale factor of a charge pump circuit, and a pressure-lowering scale factor. In the negative 6 times as many direction [as this] booster circuit explained by drawing 10 and drawing 12 , the pressure-up scale factor was being fixed 6 times. When Vcc falls [duty] to 3V in 1/240 of liquid crystal displays, on the negative 5 times as many direction [as this] pressure-up electrical potential difference (that is, VEE=-12V), the reason for having increased the pressure-up scale factor 6 times has insufficient VEE, and it is because about -13.5V is needed. VEE which is needed in the same liquid crystal display is abbreviation-10.5V, when Vcc is 3.3V and abbreviation-12V and Vcc are 3.6V. The reason VEE(s) which are needed with the electrical potential difference of Vcc differ is as follows. That is, in this example, Vcc, and its 1 / 2 pressure-lowering electrical potential differences are used as it is as an electrical potential difference which drives X electrode. Therefore, if Vcc becomes high, the effective voltage which joins liquid crystal at a non-selection period needs to become high, and needs to make small the part and a selection electrical potential difference. Conversely, it is because the effective voltage which joins liquid crystal at a non-selection period also needs to become low and needs to enlarge the part and a selection electrical potential difference, if Vcc becomes low. The direction 5 times instead of 6 times are enough as when the pressure-up scale factor of Vcc of the negative 6 times as many direction [as this] booster circuit 2 of drawing 1 is higher than 3.3V, cuts automatically 5 times from the above reason when Vcc is high rather, and it was made to change becomes small and has desirable power consumption. Moreover, even when Vcc falls to 3V in the liquid crystal display of 1/200 duty, the negative 5 times as many direction [as this] pressure up is enough. For this reason, it is desirable that it can be made to perform the change to 5 times with an external terminal from the change to 5 times to 6 times and 6 times.

[0117] Modification of a pressure-up scale factor and a pressure-lowering scale factor is realizable as follows. For example, what is necessary is just to make it a configuration like drawing 26 , in order to enable modification of a pressure-up scale factor in the circuit shown in above-mentioned drawing 10 . Namely, what is necessary is to form the scale-factor modification circuit 20, to connect the contact A of SWa2 at -V3B in the case of a 6 time pressure up, and just to connect the contact A of SWa2 at GND in the case of a 5 time pressure up. Or the scale-factor modification circuit 22 may be formed, in the case of a 6 time pressure up, the contact B of SWb2 may be connected at -V3B, and, in the case of a 5 time pressure up, the contact B of SWb2 may be connected at GND. What is necessary is on the other hand, just to make it a configuration like drawing 27 , in order to enable modification of a pressure-up scale factor in the circuit shown in above-mentioned drawing 12 . Namely, what is necessary is to form the scale-factor modification circuit 24, to connect the contact A of SWa2 at -V3B in the case of the negative 6 times as many direction [as this] pressure up, and just to connect the contact A of SWa2 at GND in the case of the negative 5 times as many direction [as this] pressure up.

[0118] Moreover, what is necessary is just to perform as follows 3 / 2 double pressure up, for changing into pressure lowering 2/3 time. Namely, what is necessary is just to establish a change means which connects + terminal of Cb to Vcc and connects - terminal to an output terminal for this as shown in drawing 16 (A) and drawing 16 (B) in 3 / 2 double booster circuit shown in drawing 14 (A) and drawing 14 R> 4 (B), although an output terminal is connected to + terminal of Cb and Vcc is connected to - terminal.

[0119] Thus, according to this example, the charge pump circuit which performs a pressure up, L/M twice (however, L/M is not integer) pressure lowering, or charge pump actuation of a M/L time pressure up K times (K>=2), and a means to change the pressure-up scale factor or pressure-lowering scale factor of this charge pump circuit are established. The current vainly consumed by the contrast

equalization circuit 3 grade of drawing 1 can be reduced by this, and further low-power-ization can be attained.

[0120] In addition, −V3B is formed and this −V3B is equivalent to the pressure up electrical potential difference on the basis of Vcc in the negative 6 times as many direction [as this] booster circuit shown in drawing 10 and drawing 12 twice in the negative direction in GND. On the other hand, it is the output voltage of the negative direction 2 double booster circuit 5 of drawing 1 . − V3 is equivalent to the pressure up electrical potential difference on the basis of Vcc twice in the negative direction in GND. It is the output voltage of the negative direction 2 double booster circuit 5, without preparing the circuit which follows, for example, consists of SWb1, SWa1, Cp1, and Cp2 in drawing 10 and drawing 12 . − They are drawing 10 and drawing 12 about V3. − Using in common as V3B is also possible. Or it is also possible to share −V3B of the negative 6 times as many direction [as this] booster circuit 2 as −V3 conversely, without forming the negative direction 2 double booster circuit 5. However, since the fall of the output voltage by the load current becomes large in using in common, it is desirable to use properly whether according to panel size, it uses in common.

[0121] [Example 6] An example 6 is an example which established a means to stop supply of the high voltage by the given period after the injection of an input power electrical potential difference, and the charge pump circuit.

[0122] When generating the high voltage (the 1st potential VH of drawing 1 R> 1, the Nth potential VL) using a charge pump circuit, unless it suspends the given period after the injection of an input power electrical potential difference, and generating of the high voltage, a system may not start normally. One of the reason of the is because the output circuit inside a driver IC etc. may be in a short condition if the logic part of a driver IC (a data-line driver, scanning-line driver) is not operating normally before the high voltage occurs. In order to prevent such a situation, as shown in drawing 28 (A), the supply interruption circuit 26 is formed in the negative 6 times as many direction [as this] booster circuit 2 of drawing 1 . And what is necessary is just to intercept between the given period after the injection of an input power electrical potential difference, and −V3Bin(s) and −V3Bout(s). An example of the concrete configuration of this supply interruption circuit 26 is shown in drawing 28 (B). After Vcc is supplied, the given period decided by the time constant of CxR and Tr turn off, and between −V3Bin and −V3Bout(s) is intercepted. Furthermore, it is desirable to insert resistance of about 10ohms in the path between the path between Vcc of the path which uses an input power electrical potential difference as output voltage of a power circuit as it is, i.e., drawing 1 , and V3 and GND, and VC as an object for overcurrent protections.

[0123] In addition, with the configuration of drawing 1 , if supply of VL (the Nth potential) is suspended by the supply interruption circuit 26 prepared in the negative 6 times as many direction [as this] booster circuit 2, supply of VH (the 1st potential) will also be suspended. It becomes unnecessary therefore, to prepare a supply interruption circuit in the 2 double booster circuit 4. What is necessary is on the other hand, just to prepare a supply interruption circuit in this 6 time booster circuit, in supplying VH using the pressure up circuit [Vcc] on the basis of GND 6 times.

[0124] [Example 7] The block diagram of the power circuit of an example 7 is shown in drawing 29 . This power circuit has the function to generate the electrical potential difference on which only Vcc−GND was, on the whole, able to shift the output voltage of the power circuit of the example 1 shown in drawing 1 to the high potential side. In the example 1 of drawing 1 , although the 1st − the Nth potential were formed in the symmetry to the 2nd input potential GND by the side of low voltage, they are formed in the symmetry by drawing 29 to the 1st input potential Vcc by the side of high potential.

[0125] In order to simplify explanation, only a different part from an example 1 is mainly explained. The negative 5 times as many direction [as this] booster circuit 32 generates the pressure up electrical potential difference [GND] VEE on the basis of Vcc by charge pump actuation 5 times in the negative direction. VEE is set to −13.2V when Vcc is 3.3V. The 2 double booster circuit 34 generates the 2

double pressure up electrical potential difference [Vcc] VH on the basis of VL. The 2 double booster circuit 35 generates the 2 double pressure up electrical potential difference [Vcc] V3 on the basis of GND. 1 / 2 double pressure-lowering circuits 36 and 37 are V2 which is the electrical potential difference which divided between V3-Vcc into two equally, and the electrical potential difference which divided between Vcc-GND into two equally. - V2 is generated. The electrical potential difference which drives a liquid crystal panel above has been formed. In addition, GND is used for -V3 as it is at VC of central potential, using Vcc as it is. This power circuit is equipped with the description of [to the input power electrical potential difference Vcc by the side of high potential] the symmetry in the level of the electrical potential difference outputted. According to the power circuit of such a configuration, low-power-ization of the liquid crystal display driven with four-line coincidence sorting by selection is attained for the same reason as the reason explained in the example 1.

[0126] Thus, when output voltage required for a liquid crystal drive has main potential and a great portion of consumed electric current flows between the main potential and other electrical potential differences, main potential is made in agreement with the 1st and 2nd input potential, and low-power-ization of a liquid crystal display can be attained by using the configuration of forming output voltage in the circuit which made the charge pump circuit the subject. According to such a configuration, since the consumed electric current in high voltages VH and VL becomes small, these high voltages VH and VL can be formed easily in the low charge pump circuit of output capacity. And further low-power-ization of a liquid crystal display can be attained by forming these high voltages in the small charge pump circuit of power loss.

[0127] In addition, in an example 7, after changing the negative 5 times as many direction [as this] booster circuit into the booster circuit of the forward direction and forming VH in a contrast equalization circuit, it is also possible to carry out 2 double pressure up of the VH in the negative direction, and to form VL.

[0128] [Example 8] The block diagram of the power circuit of an example 8 is shown in drawing 30 . This power circuit has the function to generate the electrical potential difference on which only 1/2x (Vcc-GND) was, on the whole, able to shift the output voltage of the power circuit of an example 1 to the high potential side. In the example 8, the 1st - the Nth potential are formed in the symmetry on the basis of the middle point potential of the 1st input potential Vcc and the 2nd input potential GND.

[0129] 1 / 2 pressure-lowering circuits 46 are circuits which generate the electrical potential difference VC which divided between Vcc-GND into two equally by charge pump actuation, and this VC serves as main potential of the 1st - the Nth potential. The negative 5 times as many direction [as this] booster circuit 42 generates the pressure up electrical potential difference [GND] VEE on the basis of Vcc 5 times in the negative direction. The 2 double booster circuit 44 generates the 2 double pressure up electrical potential difference [VC] VH on the basis of VL. The negative direction 2 double booster circuit 45 is a 2 double pressure up electrical potential difference [GND / direction / negative] on the basis of VC. - V3 is generated. The 2 double booster circuit 49 generates the 2 double pressure up electrical potential difference [Vcc] V3 on the basis of VC in the forward direction. The electrical potential difference which drives a liquid crystal panel above has been formed. In addition, GND is used for -V2 as it is V2, using Vcc as it is. This power circuit is equipped with the description of [to the middle point potential VC of the 1st input potential and the 2nd input potential] the symmetry in output voltage. According to the example 8, low-power-ization of the liquid crystal display driven with four-line coincidence sorting by selection is attained for the same reason as the reason explained in the example 1.

[0130] In addition, when a desired electrical potential difference is 5 level, it is good also as a configuration which omits the 2 double booster circuit 49 and the negative direction 2 double booster circuit 45 in drawing 30 .

[0131] [Example 9] The block diagram of the power circuit of an example 9 is shown in drawing 31 . In

the example 9, the output voltage of a power circuit is formed in the symmetry to the middle point potential of the 1st and 2nd input potentials Vcc and GND. Moreover, the power circuit of an example 9 is a circuit which drives the liquid crystal panel which used 2-terminal mold nonlinear switching element. The power circuit of an example 9 outputs the working voltage which is not shaken to the power circuit explained by drawing 51 being the method which shakes the supply voltage applied to Y driver. The example of a panel drive wave when using this power circuit for drawing 32 is shown.

[0132] Drawing 32 is explained previously first. VSH is a selection electrical potential difference by the side of forward, and VSL is the selection electrical potential difference of a negative side. VNH is the non-choosing electrical potential difference after choosing VSH, and VNL is the non-choosing electrical potential difference after choosing VSL. There is relation to each electrical potential difference it is unrelated VSH-VNH=VNL-VSL that the middle point potential of VNH and VNL is equal to the middle point potential of VSH and VSL if it is related and puts in another way. An axis of abscissa t is a time-axis, and 1 graduation is equivalent to die-length t1H of one selection period. A train electrode drive wave is an example in case a gradation means is pulse width gradation. The configuration of a power circuit becomes it is remarkable and easy by making the electrical potential difference which drives a train electrode in agreement with the non-choosing electrical potential difference of a line electrode like drawing 32 .

[0133] Next, the circuit of drawing 31 is explained. It is a non-choosing electrical potential difference and Vcc and GND of the electrical potential difference for a logic drive are used for coincidence as it is at VNH and VNL which are also train electrode driver voltage. The negative 5 times as many direction [as this] booster circuit 52 generates the pressure up electrical potential difference [GND] VEE on the basis of Vcc 5 times in the negative direction. VEE is set to -20V when Vcc is 5V. A booster circuit 60 carries out the pressure up of the same electrical-potential-difference difference as VNL-VSL on the basis of VNH, and generates VSH. The electrical potential difference which drives a liquid crystal panel above has been formed. The power circuit of this configuration is equipped with the description of [to the middle point potential of the 1st and 2nd input potential] the symmetry in output voltage.

[0134] Although the operating voltage of a power circuit or Y driver will shake and it will become high to about twice compared with the case where it is a power-source method if the liquid crystal panel using 2 terminal mold nonlinear switching element is driven by the power circuit of the above-mentioned configuration, the power consumption of a liquid crystal display can be reduced. Since one of the reason of the has the static electrical potential difference which has joined Y driver, it is for the trouble which happened by the shaking power-source method not to arise. That is, the trouble of carrying out charge and discharge by the electrical-potential-difference width of face by which the holoparasitism capacity of Y driver is shaken, and the trouble that a current flows in short within Y driver in the timing shaken do not arise in this example. Since the charge and discharge current and the short current of a high-voltage system of Y driver in one selection period happen only by one in the output which has hundreds of even if the high voltage turns into a twice [about] as many electrical potential difference as this, the increases of a current by high-voltage-izing are very few. Another reason is because the power consumption of the power circuit itself is very small. This depends output voltage on generating in the booster circuit of the high charge-pump type of effectiveness. According to this example, it became possible to drive the liquid crystal panel using 2 terminal mold nonlinear switching element by the power consumption of the abbreviation one half of a shaking power-source method.

[0135] In addition, by this example, it has explained using the negative 5 times as many direction [as this] booster circuit 52. However, what is necessary is just to let the negative 5 times as many direction [as this] booster circuit 52 be the negative 4 times as many direction [as this] booster circuit, when you use low-battery liquid crystal. Moreover, while lowering Vcc to 3.3V, it is good if needed also considering the negative 5 times as many direction [as this] booster circuit 52 as a negative 6 times as many direction [as this] booster circuit. Moreover, although explained by this

example that the gradation display means was based on the Pulse-Density-Modulation method, the inter-frame lengthening method may be used.

[0136] Moreover, when a desired electrical potential difference is 5 level, in drawing 31 , 1 / 2 double pressure-lowering circuit may be added to between VCC-GND, and central potential may be generated.

[0137] [Example 10] The block diagram of the power circuit of an example 10 is shown in drawing 33 . Unlike an example 9, in the example 10, VNL which are the 1st and 2nd input potentials Vcc and GND and different potential is generated. And the output voltage of a power circuit is formed in the symmetry to middle point potential with this VNL, Vcc, or GND.

[0138] In the example 10, Vcc of the electrical potential difference for a logic drive is used for VNH which is a non-choosing electrical potential difference and is also train electrode driver voltage as it is. Negative direction 3 / 2 double booster circuit 61 generates the 2 double pressure up [3 /] electrical potential difference [GND] VNL on the basis of Vcc in the negative direction. The example of a configuration of negative direction 3 / 2 double booster circuit 61 is as drawing 15 (A) and drawing 15 (B) having already explained. The negative 5 times as many direction [as this] booster circuit 62 generates the pressure up electrical potential difference [VNL] VEE on the basis of Vcc 5 times in the negative direction. When Vcc is 3.3V, Vcc-VNL is set to 4.95V, VNL-VEE is set to 19.8V, and output voltage almost equal to the case where Vcc is 5V is obtained in an example 9. A booster circuit 70 carries out the pressure up of the same electrical-potential-difference difference as VNL-VSL in the forward direction on the basis of VNH, and generates VSH. The electrical potential difference which drives a liquid crystal panel above has been formed. This power circuit generated the 1st and 2nd input potential and different potential VNL in the charge pump circuit, and output voltage is equipped with the description of the symmetry to the middle point potential of Vcc and VNL. According to the example 10 of the above configuration, since a logic electrical potential difference is made to a low battery, the liquid crystal panel using 2 terminal mold nonlinear switching element can be further driven with a low power rather than an example 9.

[0139] [Example 11] The block diagram of the power circuit of an example 11 is shown in drawing 34 . Differing from the example 1 shown in drawing 1 is the point that an input power electrical potential difference contains the 3rd input potential Vee, in the example 11. That is, in the example 11, it has 2 power-source composition (Vee, Vcc, GND) to having been a single power supply configuration (Vcc, GND) in the example 1.

[0140] The negative direction 2 double booster circuit 72 generates the 2 double pressure up electrical potential difference [GND] VL on the basis of the 3rd input potential Vee by charge pump actuation in the negative direction. The negative direction 2 double booster circuit 73 is a 2 double pressure up electrical potential difference [GND / direction / negative] on the basis of the 1st input potential Vcc. - V3 is generated. 1 / 2 pressure-lowering circuits 74 and 75 are the electrical potential difference V2 which divided between Vcc-GND into two equally, and the electrical potential difference which divided between GND- (- V3) into two equally. - V2 is generated. Moreover, GND is used for VC as it is V3, using Vcc as it is. An electrical potential difference required of for example, four-line coincidence sorting by selection can be formed by the power circuit of the above configuration. In addition, it is as drawing 9 having already explained the configuration of 1 / 2 pressure-lowering circuits of a charge pump method.

[0141] The block diagram at the time of establishing 1 / 3 pressure-lowering circuits 76 and 77 in drawing 35 instead of 1 / 2 pressure-lowering circuits 74 and 75 is shown. 1 / 3 pressure-lowering circuits 76 and 77 are the electrical potential differences V1 and V2 which divided between Vcc-GND every [3 / 1/], and the electrical potential difference which divided between GND- (- V3) every [3 / 1/] respectively. - V1 and -V2 are generated. By this power circuit, an electrical potential difference required of for example, six-line coincidence sorting by selection can be formed.

[0142] In addition, this example has described the case where both Vee and Vcc are forward potentials,

to GND so that it may be easy to understand, but neither Vee nor Vcc needs to be forward potential, and as shown in drawing 36 , both Vee, and both [one side or] may be negative potential to GND.
[0143] This example explained above has the description on the following configurations.
[0144] That is, in this example, the 1st input potential Vcc by the side of the high potential contained in an input power electrical potential difference and the 2nd input potential GND by the side of low voltage are used as it is as the Gth potential V3 in the 1st − the Nth potential (N>=4), and the Jth potential VC. Moreover, the 3rd input potential Vee by the side of high potential or low voltage is used rather than the 1st and 2nd input potential as the 1st potential VH by the side of high potential, or the Nth potential VL by the side of low voltage. Moreover, the charge pump circuit which performs charge pump actuation based on a given clock, and supplies directly either of the 1st and Nth potential VH and VL through an adjustment means (negative direction 2 double booster circuit 72), The charge pump circuit (negative direction 2 double booster circuit 73) which supplies directly the Fth potential by the side of high potential or low voltage (1<F<N) through an adjustment means rather than the Gth and Jth potential is included. And potentials other than said 1st, Fth, Gth, Jth, and Nth potential in the 1st − the Nth potential are further supplied by the charge pump circuit (1 / 2 pressure−lowering circuits 74 and 75, 1 / 3 pressure−lowering circuits 76 and 77) which carries out charge pump actuation based on a given clock. According to the above configuration, although the 1st potential VH or the Nth potential VL of output capacity which does not need output capacity so much is low, while being supplied in an efficient charge pump circuit, the Gth potential V3 and the Jth potential VC are connected to the high input power electrical potential differences Vcc and GND of output capacity. Furthermore, the electrical potential difference of V2 and −V2 grade is supplied in a charge pump circuit. Thereby, it is compatible in maintenance and low−power−izing of display quality. In addition, the configuration of this example also has the description on the configuration that charge pump circuits, such as the description on the configuration explained by (3) of an example 1, i.e., a K time pressure up, and L/M twice pressure lowering, are intermingled.
[0145] Next, the power consumption of this example is explained. According to [in the consumed electric current of the V3−VC system of the load circuit located in the latter part from a power circuit] Id, then this example for the consumed electric current of Ic and a −V3−VC system, the power consumption by Ic serves as IcxVcc. Moreover, the power consumption by Id serves as IdxVcc mostly by making the negative direction 2 double booster circuit 73 into an efficient booster circuit. On the other hand, in the power circuit of drawing 49 , the power consumption by Ic is IcxVEE and the power consumption by Id serves as IdxVEE. If Vcc=5V and VEE=20V, the power consumption of the power circuit of drawing 49 is set to x(Ic+Id)20V, and the power consumption of this example is set to x(Ic+Id)5V. Therefore, power consumption can be reduced to 4 by about 1/.
[0146] Moreover, although the above has been described only paying attention to intermediate voltage, it can say that the same is said of the power consumption in VH or VL. That is, the power consumption according the consumed electric current of the Ia and VL−VC systems to Ib, then Ia and Ib in the consumed electric current of the VH−VC system of the load circuit located in the latter part from a power circuit becomes x20V in the power circuit of drawing 49 (Ia+Ib). On the other hand, in this example, by making the negative direction 2 double booster circuit 72 into an efficient booster circuit, power consumption is set mostly (Ia+Ib) to x10V, and can carry out an abbreviation reduction by half. When a load circuit needs a main electrical potential difference and a great portion of consumed electric current flows between the main electrical potential difference and other electrical potential differences, large low−power−ization of this example is attained so that the above explanation may show.
[0147] In addition, in the example 11, LP which is a pulse−like clock can generate a clock like an example 1, and charge pump actuation can be performed. Moreover, also in the example 11, the charge pump circuit of various configurations which were explained in the example 2 is employable. Moreover, the various technique that it explained in the example 3 − the example 6 can be adopted, and low−

power-ization can also be attained. Furthermore, in drawing 34 and drawing 35 , although output voltage serves as symmetry to GND, it is also possible to form output voltage in the symmetry to a middle point electrical potential difference with the symmetry, a given generated voltage, Vcc, or GND to the symmetry and the middle point electrical potential difference of Vcc and GND to Vcc. Moreover, what is necessary is to have formed 1 / 2 pressure-lowering circuits 74 and 75 in drawing 3434 , in order to obtain the electrical potential difference of 7 level, but just to omit 1 / 2 pressure-lowering circuits 74 and 75, when a desired electrical potential difference is 5 level. Furthermore, what is necessary is just to consider as a configuration as shown in drawing 2 , in performing 1/2 pressure lowering, 1/3 pressure lowering, etc. using an operational amplifier.

[0148] [Example 12] An example 12 is an example which makes the residual charge of a circuit part with which an electrical potential difference is supplied by at least one side of the 1st and Nth potential discharge, when at least one of the inputs of the supply interruption of an input power electrical potential difference, the supply interruption of a given clock, or a display off control signal is made.

[0149] When supply interruption of an input power electrical potential difference or supply interruption of a clock is performed to drawing 37 , the example of a circuit which makes the residual charge of VH and VL systems discharge is shown. In drawing 37 , a signal / A and A are the clock signals of opposition mutually. Moreover, Trp8 and Trp9 are PMOS transistors, and while the clock is supplied, one side of a transistor turned them on and they have repeated actuation that another side turns off. If Trp8 turns on, a capacitor Cc 1 will be charged on an electrical potential difference Vcc, and if TrP9 turns on, the charge of Cc1 will move to Cc2. If the time constant by Cc2 and Resistance Rc is set up more greatly enough than the period of a clock signal, the input of Buffer Buf will serve as level almost near an electrical potential difference Vcc. Since one of transistors will become surely off if a clock stops, the input of Buf serves as GND level by Rc, and the output of Buf also serves as GND level. Also when supply of an electrical potential difference Vcc stops, the input and output of Buf serve as GND level.

[0150] As for Trn5 and Trn6, an NMOS transistor, and Trp5, Trp6 and Trp7 are PMOS transistors. Ra1, Ra2, and Rb1 are resistance of about several M omega, and they are respectively set as bigger resistance than the resistance at the time of ON of Trn5 or TrP5. Therefore, even when these transistors turn on, the consumed electric current which flows through these resistance is small. Since the output of Buf is Vcc level when an electrical potential difference Vcc is supplied and the clock is supplied, Trn5 turns on. If Trn5 turns on, the gate of Trp7 will become a low side, Trp7 will turn on, and an electrical potential difference Vee will be supplied to VH. Moreover, the gate of Trn6 is set to GND level, and Trn6 turns off. Electrical potential difference - V3 is [about], while it is the reversal output of an electrical potential difference Vcc (drawing 1 , R> drawing 34 4 reference), an electrical potential difference Vcc is supplied and the clock is operating. -It has level of Vcc. Thereby, Trp5 turns on and Trp6 turns off.

[0151] When supply of an electrical potential difference Vcc stops or supply of a clock stops, it is the output and electrical potential difference of Buf. - V3 is set to GND level and turns off Trn5 and Trp5. If Trn5 turns off, the gate of Trp7 will serve as Vee level, Trp7 will turn off, and the supply to VH from Vee will be intercepted. Moreover, the gate of Trn6 also serves as Vee level, and is turned on, and the charge which remained in VH system discharges to GND through the resistance Ra 3 which is about 10Kohm. Moreover, if Trp5 turns off, the gate of Trp6 will become a low side, Trp6 will turn on, and the charge which remained in VL system will discharge to GND through the resistance Rb2 which is about 10Kohm.

[0152] As mentioned above, when supply of an electrical potential difference Vcc or a clock stops, while intercepting supply of an electrical potential difference Vee according to this example, it can realize making the residual charge of a circuit part with which an electrical potential difference is supplied by electrical potential differences VH and VL discharge, without making most power consumption increase. Thereby, the abnormality situation where the high voltage of a direct current continues being impressed

to the above-mentioned circuit part can be prevented.
[0153] The example of a circuit which makes the charge of VH and VL systems emit to drawing 38 with display ON / OFF signal is shown. The main differences with drawing 37 are the points of having inputted Signal Don into the gate of Trn5. Signal Don is a signal which controls display ON / OFF of a liquid crystal display, and it is a signal used as a low level (GND) at the time of high level (Vcc) and display OFF at the time of display ON. When Don is high-level, Trn5 turns on, the gate of Trp7 becomes a low side by this, and Trp7 turns on. Thereby, an electrical potential difference Vee is supplied to VH.
[0154] On the other hand, when Don is a low level, Trn5 turns off, the gate of Trp7 serves as Vee and this level by this, and Trp7 turns off. Thereby, supply of the electrical potential difference Vee to VH is intercepted. The gate of Trn6 also serves as Vee and this level at coincidence, and Trn6 turns on. The charge which remains in VH system by this discharges.
[0155] By inputting display ON / off control signal into the power circuit of this example as mentioned above, display ON / OFF of a liquid crystal display can be controlled easily, without making the consumed electric current increase. In addition, by the approach of adding the circuit which suspends a clock when not the approach of inputting Signal Don into the gate of Trn5 directly as mentioned above but Don is a low, the residual charge of VH system may be made to discharge and a liquid crystal display may be made into a display OFF state. Moreover, a liquid crystal display may be made into a display OFF state by controlling the reset terminal of DF, suspending a clock, as shown in drawing 4 , and stopping actuation of a charge pump circuit.
[0156] When input power turns off in drawing 39 (A) and drawing 39 (B), the example of a circuit which makes the charge of VH and VL systems discharge is shown. For example, if input power turns off in drawing 39 (A) and it becomes Vcc=GND, Trn10 will turn off and the gate of Trn11 will be on a high side. Trn11 turns on by this and the charge of VH system discharges to GND. Moreover, in drawing 3939 (B), if it becomes Vcc=GND, Trp10 will turn off and the gate of Trp11 will become a low side. Trp11 turns on by this and the charge of VL system discharges to Vcc.
[0157] When input power turns off in drawing 40 (A) and drawing 40 (B), and when a display OFF signal is inputted into them, the example of a circuit which makes the charge of VH and VL systems discharge is shown. Doff is a signal set to high level (= Vcc) at the time of display OFF. If Doff becomes high-level, /Doff which is the reversal signal serves as a low level (= GND), Trn10 will turn off by this and the gate of Trn11 will be on a high side. Trn11 turns on by this and the charge of VH system discharges to GND. Moreover, in drawing 40 (B), if Doff becomes high-level, Trp10 will turn off and the gate of Trp11 will become a low side. Trp11 turns on by this and the charge of VL system discharges to Vcc.
[0158] [Example 13] The example of a configuration of a liquid crystal display including the power circuit explained to drawing 41 in the example 1 – the example 12 is shown. This liquid crystal display contains the liquid crystal panel 88 containing the liquid crystal layer driven with two or more data-line electrodes and two or more scanning-line electrodes, a power circuit 91, the X driver IC (data-line driver) 90 that drives a data-line electrode based on the electrical potential difference supplied by the power circuit 91, and the Y driver IC (scanning-line driver) 89 which drives a scanning-line electrode based on the electrical potential difference supplied by the power circuit.
[0159] VCC-GND is the power-source input for a logic section drive of a driver IC, and VEE-GND is a high-voltage power-source input for forming a selection electrical potential difference. VEE is unnecessary when a power circuit is a configuration like drawing 1 . LP is a latch pulse for X driver ICs, and is usually used also [clock / for Y driver ICs / containing a shift register / shift]. Other timing signals and data signals have omitted the publication, in order to make drawing legible.
[0160] The example of a driver voltage wave when driving a liquid crystal panel to drawing 42 in the circuit of drawing 41 is shown. In the drive approach indicated by claim 1 of JP,57-57718,B, this drive wave is equivalent to a drive wave, when it sets up with V111=V122. It is the electrical potential difference which VH and VL are electrical potential differences applied to the scanning-line electrode

chosen, and adds VC (VM) to a non-choosing scanning-line electrode here. Moreover, Vx0 and Vx1 are ON / electrical potential differences which follow off and are applied to X electrode of an indicative data. M is a control signal for carrying out the alternating current drive of the liquid crystal, and the polarity of the electrical potential difference applied to a liquid crystal panel by the high/low of Signal M is reversed. t1H show the die length of the time amount as which one scanning-line electrode is chosen.
[0161] An electrical potential difference required for this drive approach can be formed by the power circuit explained in the example 1 – the example 12. For example, the outputs VC, VH, and VL of a power circuit 91 are used for VH and VL of VC of non-choosing level, and selection level. Moreover, V2 is used for Vx0 of an electrical potential difference which drives X electrode, and it is in Vx1. – What is necessary is just to use V2. For example, when duty is 1/240, VH is usually about 20V, and V2 is about [of the abbreviation 1/2 of logic electrical-potential-difference 3.3V] 1.6V. Therefore, the electrical potential difference which lowered the pressure of a logic electrical potential difference to one half can also be used for V2.
[0162] The logic electrical potential difference of the X driver IC 90 should just use VCC-GND as it is. What is necessary is just to use VCC-GND as it is like the gate line driver IC for the TFT panels, as a logic electrical potential difference of the Y driver IC 89, when good in the middle of driver output voltage. However, for example like the usual driver IC for STN panels, when the low of a logic electrical potential difference is in agreement with VL, it is necessary to form independently the logic electrical potential difference VDD for Y driver IC 89. Drawing 43 is the example of the logic electrical-potential-difference generating circuit for Y drivers used in this case, and carries out same actuation to the part shown in H of drawing 24 R> 4 fundamentally. That is, B is the signal shown in drawing 5 , and is a signal which drives VCC-GND as a power source. Moreover, as for diode, and Buf1 and Buf2, a buffer, and Rf1 and Rf2 are [the coupling capacitor whose capacity of Cs1 and Cs2 is about 470pF, and D1 and D2] resistance of an about [1Kohm]. One hold circuit is formed by Buf1 and Rf1, and another hold circuit is formed by Buf2 and Rf2. If it is made connection like drawing 37 R> 7 and the negative side power supply terminal of a buffer is connected to VL, in the forward side power supply terminal of a buffer, the electrical potential difference VDDy only with VCC higher than VL will occur. Therefore, what is necessary is just to use this VDDy as the power source for logic for Y driver IC 89. The clock frequency of the Y driver IC 89 is about [of the X driver IC 90] 1/80, and the consumed electric current of the logic section of the Y driver IC 89 is very small. Therefore, it can fully drive with the supply voltage formed by the above simple technique. Moreover, the circuit of drawing 43 also has the function which carries out the level shift of the signal LP, and forms the shift clock YSCL for Y drivers. In addition, it is desirable to put in the about 0.1-micro F smoothing capacitor Cx between the power supply terminals of a buffer.
[0163] VCC explained the above as 3.3V. However, it is more desirable for low-power-izing to have changed VCC into the lower electrical potential difference using the operational amplifier etc., and to perform the drive of a power circuit 91, the Y driver IC 89, and the X driver IC 90, when VCC is 5V. Moreover, what is necessary is just to use the reversal pressure-up electrical potential difference (negative direction 2 double pressure-up electrical potential difference) of VCC as Vx1, using this VCC as Vx0 as it is, when VCC is about 1.5V.
[0164] In the liquid crystal display of the above configuration, the power circuit itself is a low power. Furthermore, the charge and discharge current which occupies most panel currents, i.e., the charge and discharge current which flows between X electrode and Y electrode in the condition of not choosing, is supplied from a lower logic section driver voltage system rather than it is supplied from a high-voltage system. Therefore, the power consumption by the panel current is also reduced sharply, and can make power consumption remarkably small as a whole.
[0165] [Example 14] Other examples of a configuration of a liquid crystal display are shown in drawing 44 (A). Since it is the same configuration as an example 13 fundamentally, only a different part from an

example 13 is explained. This example is an example in the case of driving Y electrode with two-line coincidence sorting by selection.

[0166] An electrical potential difference with required in the case of this drive approach adding to a liquid crystal panel is shown in drawing 44 (B). VC (VM) which is non-choosing level, and VH and VL which are selection level are required for the drive of Y electrode like an example 13. VH and VL are in symmetric relation mutually considering VC as a core here. The electrical potential difference of 3 level of Vx0-Vx2 is required for the drive of X electrode. Vx(es)1 are VC and this potential and Vx0 and Vx2 have them in symmetric relation mutually considering Vx1 as a core. for example, the number of Y electrodes scanned in 1 frame period — about 240 — and — if VC is set to 0V when Vth (SURESSHORUDO electrical potential difference) uses about [2V] usual liquid crystal with actual value — VH — about 16 — V and Vx0 — about 2 — it is set to V. That is, different points from an example 13 are only the point that main potential is added as driver voltage of X electrode, and a point which VH falls a little and Vx0 goes up a little. The power circuit of this example is suitable for generating the electrical potential difference in such symmetric relation with a low power.

[0167] When VCC is 3.3V, Vth should just use about [1.6V] low-battery liquid crystal with actual value. Moreover, what is necessary is to use low-battery liquid crystal too and just to use this VCC as Vx0 as it is, when VCC is about 1.5V.

[0168] The power consumption by the panel current is also sharply reduced by the reason as the reason which it explained in the example 13 while the power circuit itself was a low power nil why the liquid crystal display of this example is the same. Moreover, the maximum electrical potential difference which is needed for a drive is also lower than an example 13, it ends, and further low-power-ization can be attained. Moreover, in the example of a comparison of drawing 49 , when the consumed electric current in the logic section of X driver etc. was set to IXD, the power consumption by this was IXDxVEE. On the other hand, in this example, power consumption can be managed with IXDxVCC and can attain large low-power-ization compared with the example of a comparison.

[0169] [Example 15] Other examples of a configuration of a liquid crystal display are shown in drawing 45 (A). This example is an example in the case of driving Y electrode with four-line coincidence sorting by selection.

[0170] An electrical potential difference with required in the case of this drive approach adding to a liquid crystal panel is shown in drawing 45 (B). VC which is non-choosing level, and VH and VL which are selection level are required for the drive of Y electrode, and VH and VL are in symmetric relation mutually considering VC as a core. The electrical potential difference of 5 level of Vx0-Vx4 is required for the drive of X electrode, and Vx(es)2 are VC and this potential. Vx0, Vx4, and Vx1 and Vx3 are in symmetric relation mutually considering Vx2 as a core, and they satisfy Vx0-Vx1=Vx1-Vx2=Vx2-Vx3=Vx3-Vx4. For example, the number of Y electrodes scanned in 1 frame period is about 240, and when Vth uses about [2V] usual liquid crystal with actual value, if the electrical potential difference of VC is set to 0V, VH will be set to about 11.3v and Vx0 will be set to about 2.9 V. That is, different points from an example 14 are only the point that the electrical potential difference of 2 symmetrical level is mutually added to main potential as driver voltage of X electrode, and a point which VH falls a little and Vx0 goes up a little.

[0171] Since VCC and Vx0 are comparatively near level especially when VCC is 3.3V, it is possible to use VCC also as Vx0 as it is, as shown in drawing 45 (A). In this case, contrast adjustment can also be made easy, if VEE is set up a little low and Vth grazes it, using a little high liquid crystal.

[0172] [Example 16] Other examples of a configuration of a liquid crystal display are shown in drawing 46 (A). This example is an example in the case of driving Y electrode with six-line coincidence sorting by selection.

[0173] An electrical potential difference with required in the case of this drive approach adding to a liquid crystal panel is shown in drawing 46 (B). VC which is non-choosing level, and VH and VL which are

selection level are required for the drive of Y electrode, and VH and VL have them in it mutually considering VC as a core at symmetric relation. The electrical potential difference of 7 level of Vx0–Vx6 is required, Vx(es)3 are VC and this potential, and Vx0–Vx6 are satisfied with the drive of X electrode of Vx0–Vx1=Vx1–Vx2=Vx2–Vx3=Vx3–Vx4=Vx4–Vx5=Vx5–Vx6. for example, the number of Y electrodes scanned in 1 frame period — about 240 — and -- if the electrical potential difference of VC is set to 0V when Vth uses about [2V] usual liquid crystal with actual value — VH — about 9.2 — V and Vx0 – – about 3.6 — it is V. That is, different points from an example 15 are only the point that the electrical potential difference of 2 symmetrical level is mutually added to main potential as driver voltage of X electrode, and a point which VH falls a little and Vx0 goes up a little.
[0174] Since VCC and Vx0 are comparatively near level when especially VCC is 3.3V, it is possible to use VCC also as Vx0 as it is, as shown in drawing 46 (A). In this case, contrast adjustment can also be made easy, if VEE is set up a little highly and Vth grazes it, using a little low liquid crystal.
[0175] It describes below whether the number of Y electrodes chosen as coincidence is practical even how. For example, when the number of Y electrodes scanned in 1 frame period is about 240 and the number of Rhine which makes coincidence selection is 15 – 16, the maximum electrical–potential–difference width of face required for the drive of Y electrode and the maximum electrical–potential–difference width of face required for the drive of X electrode become equal. When Vth uses about [2V] usual liquid crystal with actual value, this electrical potential difference becomes a little less than [6V]. That is, the maximum electrical potential difference for which the drive approach with many [the number of coincidence selection Rhine] Y electrodes chosen as coincidence in the 16 or less range is needed will be low, will end, and will be advantageous to reduction of power consumption at the point. However, since X driver IC also becomes cost quantity while the number of level of an electrical potential difference required for a drive increases conversely and a power circuit is complicated, it can be said that the number of Rhine which makes coincidence selection is [eight or less] practical.
[0176] In the example 13 described above – the example 16, as shown, for example in drawing 46 (A), while using the 1st and 2nd input potentials VCC and GND as V3, V2, V1, VC, –V1, –V2, or –V3 (the 1st – the Nth potential), they are used also as supply voltage of the logic section of a driver IC. The direction which prepares another supply voltage for driving the logic section of a driver IC other than the input power electrical potential difference (VEE, VCC, GND, or VCC, GND) used in a power circuit 91 is desirable at the point of driving a liquid crystal panel on the optimal electrical potential difference. However, it is not desirable for the user of a liquid crystal display that the number of input power electrical potential differences increases. Although it becomes the drive by the electrical potential difference [electrical potential difference / optimal] shifted a little even if it uses it as supply voltage of the logic section of a driver IC while using VCC and GND as V3, V2—V2, or –V3 as the example 13 – the example 16 explained, the display of the image quality which is not a problem practical is possible. Therefore, it carries out like an example 13 – an example 16, and becomes that it is more practical to suppress the increment in the number of input power electrical potential differences.
[0177] In addition, what is necessary is to generate the electrical potential difference which differs from VCC and GND by charge pump actuation, and just to use this generated voltage as V3, V2—V2, or –V3, as drawing 33 explained when there is no VCC into V3, V2—V2, and –V3 and there is no match in GND.
[0178] Moreover, as shown in drawing 41 etc., in the example 13 – the example 16, latch pulse signal LP for X drivers or the shift clock YSCL for Y drivers is used as a pulse–like clock inputted into a power circuit 91. The reason with desirable the signal which forms the clock of a power circuit 91 being a periodic pulse–like clock is as having already described the example 2. Usually, since 30 microseconds – about 100 microseconds and pulse width are the periodic pulse–like clock signals which are 100ns – about 300ns, a period can use the latch pulse signal for X drivers that there is no problem as a pulse–like clock of a power circuit 91. Although there is also a liquid crystal display into which the shift clock for Y drivers is inputted apart from the latch pulse for X drivers, since the shift clock for Y drivers in

this case is also the same periodic pulse-like clock signal as the latch pulse for X drivers, even if it uses the clock here, there is no problem. In the timing signal inputted into a liquid crystal display, these signals are the most suitable. Since the great portion of consumed electric current of a liquid crystal display is a current which flows for instead of [every] the end of 1 horizontal-scanning period, operating the charge pump circuit which supplies the current synchronizing with the latch pulse for X drivers and the shift clock for Y drivers which are a pulse-like clock for every 1 horizontal-scanning period makes sense. A period serves as pressure-up deficiency in performance from this with a long clock signal. On the other hand, although the pulse-like clock signal with a period shorter than this is desirable when securing pressure-up capacity, since such a signal is not inputted into a liquid crystal display, it is necessary to make separately, and this leads to large-scale-ization of a circuit.

[0179] [Example 17] The example which carried the liquid crystal display of this invention in drawing 47 at electronic equipment is shown. muPU (MAIKUROMAIKURO processor unit)112 controls the whole electronic equipment, and the LCD controller 113 sends out a timing signal and an indicative data required for a liquid crystal display 115. Moreover, memory (VRAM) 114 stores an indicative data and a cell 116 is the power source of electronic equipment. DC to DC converter 117 generates the high voltage required for a liquid crystal display 115 from the electrical potential difference of a cell 116. When DC to DC converter 117 may be made to build in a liquid crystal display and it makes it build in, it is desirable to use the DC-DC converter of a charge pump method like this invention. The power consumption of electronic equipment can be sharply reduced by using the liquid crystal display of this invention for such electronic equipment.

[0180] In addition, this invention is not limited to the above-mentioned example 1 - an example 17, and deformation implementation various by within the limits of the summary of this invention is possible for it.

[0181] For example, if the technique of using a pulse-like clock, the technique of changing a pressure-up scale factor, the technique of performing a charge pump for every 1 level period, etc. are power circuits not only including the power circuit of a configuration of being shown in drawing 1 , drawing 34 , etc. but the charge pump circuit which supplies the 1st - the Nth potential at least, they are variously applicable to a thing.

[0182] Moreover, it is not restricted to what also showed the configuration of a charge pump circuit to drawing 6 - drawing 24 .

[0183] Moreover, what is necessary is just to generate the clock of non overlap using a delay circuit etc., in not using LP although the above-mentioned example explained taking the case of the charge pump circuit which used the latch pulse LP.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the power circuit concerning an example 1.
[Drawing 2] It is a block diagram at the time of using an operational amplifier for generation of V2 and −V2.
[Drawing 3] It is the circuit diagram showing an example of a contrast equalization circuit.
[Drawing 4] It is the circuit diagram showing an example of a clock formation circuit.
[Drawing 5] It is a timing chart for explaining actuation of a clock formation circuit.
[Drawing 6] It is the fundamental concept Fig. of a charge pump circuit.
[Drawing 7] It is the conceptual diagram of the charge pump circuit for 2 double pressure ups.
[Drawing 8] It is the conceptual diagram of the charge pump circuit for negative direction 2 double pressure ups.
[Drawing 9] It is the conceptual diagram of 1 / charge pump circuit for 2 pressure lowering.
[Drawing 10] It is the conceptual diagram of the charge pump circuit for the negative 6 times as many direction [as this] pressure ups.
[Drawing 11] Drawing 11 (A) and drawing 11 (B) are drawings for explaining actuation of the circuit of drawing 10 .
[Drawing 12] It is the conceptual diagram of other examples of the charge pump circuit for the negative 6 times as many direction [as this] pressure ups.
[Drawing 13] Drawing 13 (A) and drawing 13 (B) are drawings for explaining actuation of the circuit of drawing 12 .
[Drawing 14] Drawing 14 (A) and drawing 14 (B) are the conceptual diagrams of 3 / charge pump circuit for 2 double pressure ups.
[Drawing 15] Drawing 15 (A) and drawing 15 (B) are the conceptual diagrams of negative direction 3 / charge pump circuit for 2 double pressure ups.
[Drawing 16] Drawing 16 (A) and drawing 16 (B) are the conceptual diagrams of the charge pump circuit for 2/3 time pressure lowering.
[Drawing 17] Drawing 17 (A) and drawing 17 (B) are the conceptual diagrams of the charge pump circuit for the negative 2/3 time as many direction [as this] pressure lowering.
[Drawing 18] It is the circuit diagram showing the example of a negative direction 2 double booster circuit.
[Drawing 19] It is drawing for explaining actuation of the circuit of drawing 18 .
[Drawing 20] Drawing 20 (A) and drawing 20 (B) are the circuit diagrams showing an example of a level shift means.
[Drawing 21] It is the circuit diagram showing an example of a charge pump circuit using diode.
[Drawing 22] It is drawing for explaining actuation of the circuit of drawing 21 .
[Drawing 23] It is the circuit diagram showing the application of the circuit of drawing 21 .
[Drawing 24] It is the circuit diagram showing the example of the charge pump circuit in which two pumping capacitors were formed.
[Drawing 25] Drawing 25 (A), drawing 25 (B), and drawing 25 (C) are drawings for explaining the technique of performing charge pump actuation for every horizontal scanning period.
[Drawing 26] It is the circuit diagram showing the example of the charge pump circuit in which the scale-factor modification section of a pressure up and pressure lowering was prepared.
[Drawing 27] It is the circuit diagram showing other examples of the charge pump circuit in which the scale-factor modification section of a pressure up and pressure lowering was prepared.
[Drawing 28] Drawing 28 (A) and drawing 28 (B) are the circuit diagrams showing the given period behind powering on, and the example which stops supply of the high voltage.
[Drawing 29] It is the block diagram of the power circuit concerning an example 7.
[Drawing 30] It is the block diagram of the power circuit concerning an example 8.

[Drawing 31] It is the block diagram of the power circuit concerning an example 9.
[Drawing 32] It is drawing showing the example of a panel drive wave.
[Drawing 33] It is the block diagram of the power circuit concerning an example 10.
[Drawing 34] It is the block diagram of the power circuit concerning an example 11.
[Drawing 35] It is the block diagram showing other examples of the power circuit concerning an example 11.
[Drawing 36] It is drawing for explaining the potential relation of an input power electrical potential difference.
[Drawing 37] It is the circuit diagram showing the example which makes the residual charge of VH and VL systems discharge.
[Drawing 38] It is the circuit diagram showing other examples which make the residual charge of VH and VL systems discharge.
[Drawing 39] Drawing 39 (A) and drawing 39 (B) are the circuit diagrams showing other examples which make the residual charge of VH and VL systems discharge.
[Drawing 40] Drawing 40 (A) and drawing 40 (B) are the circuit diagrams showing other examples which make the residual charge of VH and VL systems discharge.
[Drawing 41] It is the block diagram showing an example of the liquid crystal display concerning an example 13.
[Drawing 42] It is drawing for explaining the drive wave of the liquid crystal display of drawing 41 .
[Drawing 43] It is the circuit diagram showing an example of a level shift means.
[Drawing 44] Drawing 44 (A) is the block diagram showing an example of the liquid crystal display concerning an example 14, and drawing 44 (B) is drawing for explaining the potential relation of driver voltage.
[Drawing 45] Drawing 45 (A) is the block diagram showing an example of the liquid crystal display concerning an example 15, and drawing 45 (B) is drawing for explaining the potential relation of driver voltage.
[Drawing 46] Drawing 46 (A) is the block diagram showing an example of the liquid crystal display concerning an example 16, and drawing 46 (B) is drawing for explaining the potential relation of driver voltage.
[Drawing 47] It is the block diagram showing an example of the electronic equipment concerning an example 17.
[Drawing 48] It is the circuit diagram showing an example of the power circuit of the 1st example of a background.
[Drawing 49] It is the circuit diagram showing an example of the power circuit of the 2nd example of a background.
[Drawing 50] It is drawing showing an example of a panel drive wave for explaining the power circuit of the 3rd example of a background.
[Drawing 51] It is the circuit diagram showing an example of the power circuit of the 3rd example of a background.

[Description of Notations]

LP Latch pulse
Vcc The 1st input potential
GND The 2nd input potential
VH The 1st potential
V3 The Gth potential
VC The Jth potential
VL The Nth potential
1 Clock Formation Circuit

2 The Negative 6 Times as Many Direction [as this] Booster Circuit
3 Contrast Equalization Circuit
4 2 Double Booster Circuit
5 Negative Direction 2 Double Booster Circuit
6 1 / 2 Pressure-Lowering Circuits
7 1 / 2 Pressure-Lowering Circuits

[Translation done.]